Distribution in the UK & Ireland

Lambda Photometrics Limited
Lambda House Batford Mill
Harpenden Herts AL5 5BZ
United Kingdom
E: info@lambdaphoto.co.uk
W: www.lambdaphoto.co.uk
T: +44 (0)1582 764334
F: +44 (0)1582 712084

Operation and Service Manual

Multichannel Clock Synthesizer

CG792

Stanford Research Systems

Revision 1.00 • January 21, 2026

Certification

Stanford Research Systems certifies that this product met its published specifications at the time of shipment.

Warranty

This Stanford Research Systems product is warranted against defects in materials and workmanship for a period of one (1) year from the date of shipment.

Service

For warranty service or repair, this product must be returned to a Stanford Research Systems authorized service facility. Contact Stanford Research Systems or an authorized representative before returning this product for repair.

Stanford Research Systems, Inc.
1290–D Reamwood Avenue
Sunnyvale, CA 94089 USA
Phone: (408) 744-9040 • Fax: (408) 744-9049
www.thinkSRS.com • e-mail: info@thinkSRS.com

Printed in the U.S.A. Document Number 9-01786-903

Contents

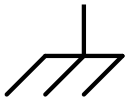
General Information

Symbols on the CG792

Warning Risk of electric shock. Injury or death is possible if the instructions are not obeyed.

Caution Refer to user manual. Damage to the instrument or other equipment is possible.

Power Toggle instrument power.



Chassis Ground

Safety and Preparation for Use

WARNING

Dangerous voltages, capable of causing injury or death, are present in this instrument. These voltages can persist for many minutes after AC power is removed. Do not remove the product covers or panels. Do not apply power or operate the product without all covers and panels in place.

AC Line Voltage

The CG792 Multichannel Clock Synthesizer operates from a 90 to 132 VAC or 175 to 264 VAC power source having a line frequency between 47 and 63 Hz. Power consumption is less than 125 W total. In standby mode, power is turned off to the main board. However, power is maintained at all times to any optional timebases installed.

Power Entry Module

A power entry module, labeled 'AC POWER' on the back panel of the CG792, provides connection to the power source and to a protective ground.

The line fuse is internal to the instrument and may not be serviced by the user.

Power Cord

The CG792 Multichannel Clock Synthesizer has a detachable, three-wire power cord for connection to the power source and to a protective ground. The chassis of the instrument is connected to the outlet ground to protect against electrical shock. Always use an outlet which has a properly connected protective ground.

BNC and SMA shields are connected to the chassis ground and the AC power source ground via the power cord. Do not apply any voltage to the shield.

Service

The CG792 Multichannel Clock Synthesizer otherwise does not have any user serviceable parts inside. Refer service to a qualified technician.

Do not install substitute parts or perform any unauthorized modifications to this instrument. Contact the factory for instructions on how to return the instrument for authorized service and adjustment.

Specifications

Valid for +20 °C to +30 °C ambient temperature.

Clock Outputs

Frequency

Range	1 mHz to 2.2 GHz
	500 Hz to 2.2 GHz (modulation enabled)
Resolution	11 digits
Setting time	< 1.0 s (typ. 0.25 s above 100 Hz)
Extra features	PRBS31 up to 100 MHz; hold High/Low

Phase

Range	± 360 deg
Resolution	
$f < 200$ Hz	$\Delta\phi \leq 30\ \mu\text{deg} \cdot f$ (Hz)
$f \geq 200$ Hz	$\Delta\phi \leq 0.01\ \mu\text{deg} \cdot f$ (Hz)
Setting time	$< 2.0\text{ s} + 2/f$
Sync abs. accuracy	< 250 ps
Sync repeatability	< 25 ps
Sync time	$3\text{ s} + 2/f$ (typ.)

Differential Outputs

Outputs	BNC
Frequency range	1 mHz to 2.2 GHz
Common-mode voltage	−3.0 V to +2.0 V
Peak-to-peak amplitude	0 V to 1.2 V
Level resolution	25 mV
Level error	$< 1\% \pm 25$ mV
Transition time	< 100 ps (20% to 80%)
Asymmetry	< 100 ps from nominal 50%
Source impedance	50 Ω ($\pm$1%)
Load impedance	50 Ω to ground on both outputs
Polarity inversion	Rear-panel BNC input
Blanking	Rear-panel BNC input
Protection	Continuous to ground, momentary to +5 VDC

Specifications (continued)

CMOS Outputs

Output	BNC
Frequency range	1 mHz to 250 MHz
Levels	0 V and 3.3 V (unterminated)
	0 V and 1.65 V (term. to 50 Ω)
Level error	< 50 mV
Transition time	< 1.0 ns (20% to 80%)
Asymmetry	< 500 ps from nominal 50%
Source impedance	50 Ω
Load impedance	50 Ω
Blanking	Rear-panel BNC input
Protection	Continuous to ground, momentary to +5 VDC

Timebase & Reference

Timebase

Stability

Std. Timebase	< 5 ppm
OCXO (Opt. 2)	< 0.01 ppm
Rb Std (Opt. 3)	< 0.0001 ppm

Aging

Std. Timebase	< 5 ppm/year
OCXO (Opt. 2)	< 0.2 ppm/year
Rb Std (Opt. 3)	< 0.0005 ppm/year

Warmup Time

OCXO (Opt. 2)	20 min
Rb Std (Opt. 3)	1 h

External Reference

In

Frequency	10 MHz
Freq. range	±10 ppm
Impedance	50 Ω
Amplitude	1–3 Vpp

Out

Frequency	10 MHz
Amplitude	2 V_{pp} sine
Impedance	50 Ω

Specifications (continued)

Noise & Spurs*

Phase noise	
100 Hz offset	< -90 dBc/Hz
1 kHz offset	< -100 dBc/Hz
10 kHz offset	< -100 dBc/Hz
100 kHz offset	< -110 dBc/Hz
vs freq.	+6 dB/oct.
Spurious	< -70 dBc (within 50 kHz of carrier)

**These values are quoted for a 100 MHz carrier. Spurs, phase noise and residual FM scale by 6 dB/octave to other carrier frequencies.*

Jitter & Wander

Jitter (rms)	$<$ 1 ps (1 kHz to 5 MHz bandwidth)
Wander (p–p)	$<$ 20 ps (10 s persistence)

Modulation

Internal Frequency Modulation (FM)

Waveforms	Sine, Triangle, Square, Noise
Period	0.1 ms to 5 s (except noise)
Dev Range	0 to 75 ppm of carrier
Dev. accuracy	$<$ ($\pm$2% of set value) $\pm$ 1 ppm
Sample rate	
Sin/Tri/Sqw	500 kSPS (fixed)
Noise	12 mSPS to 250 kSPS (adj.)

Internal Jitter Modulation

Dev Range	0 to 3 ms peak-to-peak
Sample rate	12 mSPS to 250 kSPS (non-adj.)
Dev. accuracy	$<$ $\pm$10% of set value

Specifications (continued)

Rear-Panel Analog Input

Connector	BNC, DC coupled, 1 MΩ
Input range	±1.0 V
Bandwidth	DC to 35 kHz (−3 dB)
Targets	Frequency (FM) or phase (PM)
Sample rate	1 kSPS to 250 kSPS (adjustable)
Dev Range	
FM	0 to 75 ppm/V
PM	37.5 ns/V / Sample rate (kSPS)
Dev. accuracy	< (±5% of set value) ± 1 ppm

Phase Drift (at 135 MHz carrier)

FM (Sine, Tri., Square)	< 1 ns / day
Jitter, Ext PM	< 1 ns / min

Rear-Panel Digital Input

Connector	BNC, DC coupled, 1 MΩ
Input range	0 V to 3.3 V
Input range	DC to 35 MHz
Active	HIGH
Targets available:	
Output blanking	
Polarity inversion (Diff only)	
Modulation On/Off	

Specifications (continued)

General

Interfaces	Ethernet, USB, RS-232
Line power	90 to 264 VAC, 47 Hz to 63 Hz
Standby power	
Std. Timebase	< 5 W
OCXO (Opt. 2)	< 15 W
Rb Std (Opt. 3)	< 75 W
Operating power	
Std. Timebase	< 60 W
OCXO (Opt. 2)	< 75 W
Rb Std (Opt. 3)	< 125 W
Operating	+5 °C to +40 °C
Storage	−20 °C to +70 °C
Humidity	up to 80% RH, non-condensing
Dimensions	8″ × 3.5″ × 13.5″
Weight	< 9 lbs
Warranty	One year parts and labor on defects in materials and workmanship

Remote Commands

This is the list of all remote commands accepted by the CG792. Each command is shown with the range of arguments, if any, and a brief description. See detailed command description starting on page 60.

IEEE 488.2 Common Commands

See section 3.5.1 on page 60 for details.

*CLS	Clear status registers
*ESE[?]	Set/query event status enable mask
	0 to 127
*ESR?	Read and clear event status register
*IDN?	Identify instrument
*OPC[?]	Set/query operation complete flag
*RCL	Recall stored state
	0 to 8
*RST	Reset instrument to factory defaults
*SAV	Save current state
	0 to 7
*SRE[?]	Set/query service request enable mask
	0 to 127
*STB?	Read status byte register
*TST?	Self-test query
*WAI	Wait until operations complete

Error & Info

See section 3.5.2 on page 64 for details.

`SYSTem:REBoot`	Reboot the instrument
`SYSTem:ERRor:CLEAR`	Clear error queue
`SYSTem:ERRor[:NEXT]?`	Query next error in queue
`SYSTem:FACToryreset`	Factory reset
`SYSTem:INFO:MEMory?`	Query memory usage
`SYSTem:INFO:TEMPerature?`	Query internal temperature
`SYSTem:INFO:UPTime?`	Query system uptime
`SYSTem:INFO:VOLTage?`	Query supply voltages
`SYSTem:BEEP[?]`	Set/query beep loudness
	`OFF, LOW, HIGH`

Source

See section 3.5.3 on page 68 for details.

`SOURce#:FREQuency[?]`	Set/query output frequency
	`1e-3` to `2.2e9`
`SOURce#:FASTfrequency[?]`	Set frequency faster
	`1e-3` to `2.2e9`
`SOURce#:INST?`	Query installed source module
`SOURce#:EXTPhase?`	Query phase precisely
`SOURce#:PHASe[?]`	Set/query phase
	`-720` to `720`
`SOURce#:REL`	Define current phase to be zero
`SOURce#:STATe[?]`	Enable/disable/query output
	`OFF, ON, INV, BLANK, PRBS, LOW, HIGH`
`SOURce#:SYNC`	`Align phase of outputs`
	`1, 2, 3, 4`
`SOURce#:VOLTage:AMPLitude[?]`	Set/query amplitude
	`0` to `1.2`
`SOURce#:VOLTage:OFFSet[?]`	Set/query DC offset
	`-3` to `2`

Modulation

See section 3.5.4 on page 72 for details.

`MODulation:MODE[?]`	Set/query mod mode
	`OFF, FM, PM, JITTER`
`MODulation:PERiod[?]`	Set/query mod period
	`0.1e-3` to `5`
`MODulation:PERiod:ACTual?`	Query effective period
`MODulation:BLANk[?]`	Enable/disable/query blanking
	`ON, OFF`
`MODulation:POLarity[?]`	Set/query mod polarity
	`0 or 1`
`MODulation:RATE[?]`	Set/query mod sample rate
`MODulation:TYPE[?]`	Set/query mod type
	`SINe, TRIangle, RAMP, SQUARE, NOISE, EXTernal`

Modulation (cont'd)

`SOURce#:MODulation:DEViation[?]`	Set/query mod deviation
	`0` to `75e-6`
`SOURce#:MODulation:JITTer[?]`	Set/query jitter enabled/disabled
	`ON, OFF`
`MODulation:JITTer[?]`	Set peak-to-peak jitter magnitude in seconds
	`0` to `3e-3`
`MODulation:ZERO`	Immediately pause (1) or resume (0) modulation
	`0, 1`

Communication

See section 3.5.5 on page 77 for details.

`SYSTem:COMMunicate:LAN:DHCP[?]`	Enable/disable/query DHCP
	`ON, OFF`
`SYSTem:COMMunicate:LAN:DHCP:STATus?`	Query DHCP lease status
`SYSTem:COMMunicate:LAN:IPADdress[?]`	Set/query IP address
	`0.0.0.0` to `255.255.255.255`
`SYSTem:COMMunicate:LAN:MAC?`	Query MAC address
`SYSTem:COMMunicate:LAN:RESet`	Reset LAN interface
`SYSTem:COMMunicate:LAN:STATus?`	Query LAN link status
`SYSTem:COMMunicate:SERial:BAUD[?]`	Set/query serial baud rate
	`9600` to `115200`
`SYSTem:COMMunicate:USB:BAUD?`	Query USB virtual COM baud

Display Backlight

See section 3.5.6 on page 79 for details.

`SYSTem:DISPlay:LEVel[?]`	Set/query display brightness
	`20` to `100`
`SYSTem:DISPlay:OFF[?]`	Turn display on/off
	`OFF, ON, MIN, 1H, 2H, 4H, 8H, DAY, WEEK`

Timebase / Reference

See section 3.5.7 on page 80 for details.

`SYSTem:REFerence:LOCK?`	Query reference lock status
`SYSTem:REFerence:EXTernal:STATus?`	Query external ref voltage
`SYSTem:REFerence:INTernal:TYPe?`	Query internal ref type
`SYSTem:REFerence:OCXO:FCONtrol[?]`	Set/query OCXO frequency trim `-0.4e-6` to `+0.4e-6`
`SYSTem:REFerence:OCXO:AGC?`	Query OCXO AGC status
`SYSTem:REFerence:OCXO:HEAT?`	Query OCXO heater status
`SYSTem:REFerence:OCXO:VARac?`	Query OCXO varactor status
`SYSTem:REFerence:RB:FCONtrol[?]`	Set/query rubidium frequency trim `-2e-9` to `2e9`
`SYSTem:REFerence:RB:STATus?`	Query rubidium status code
`SYSTem:REFerence:RB:TEMP#?`	Query rubidium temperature sensor
`SYSTem:REFerence:TCXO:FCONtrol[?]`	Set/query TCXO frequency trim `-49999e-9` to `49999e-9`

Performance Figures

Note: The data shown in the following figures are typical measurements and are not to be interpreted as specifications.

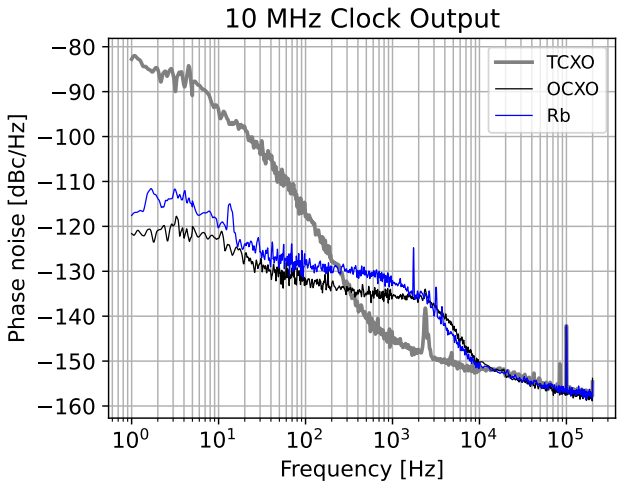


Figure 1: Phase-noise spectra of the 10 MHz clock output for three reference sources, showing their relative noise performance across offset frequency.

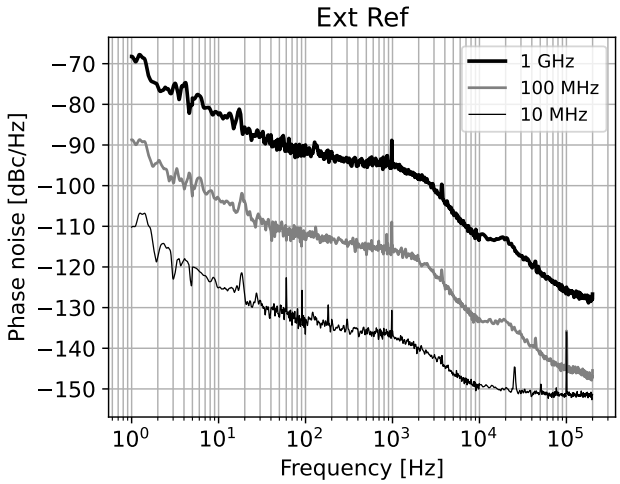


Figure 2: The phase curves (shown here at 10 MHz, 100 MHz, and 1 GHz) may be scaled by 20 dB/decade to estimate the phase noise at other frequencies.

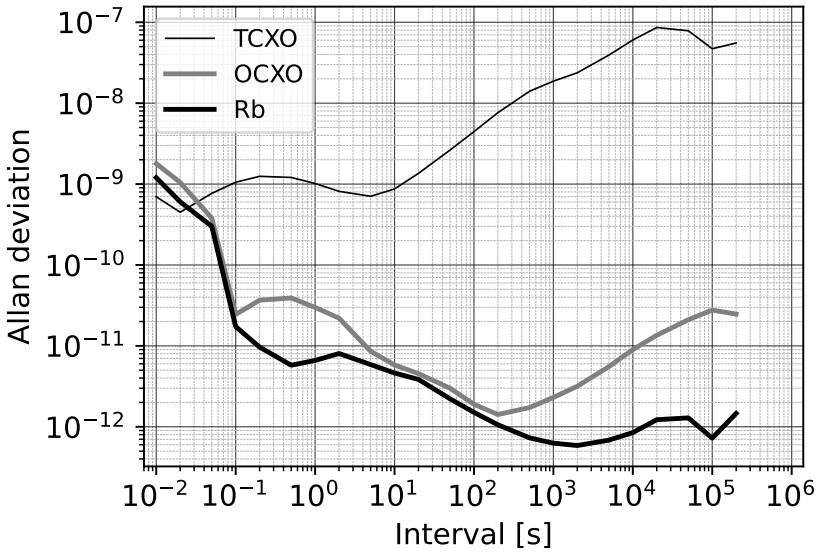


Figure 3: Allan deviation of three reference oscillators (TCXO, OCXO, and rubidium). Lower values indicate better frequency stability; different slopes correspond to noise processes dominating at different averaging intervals.

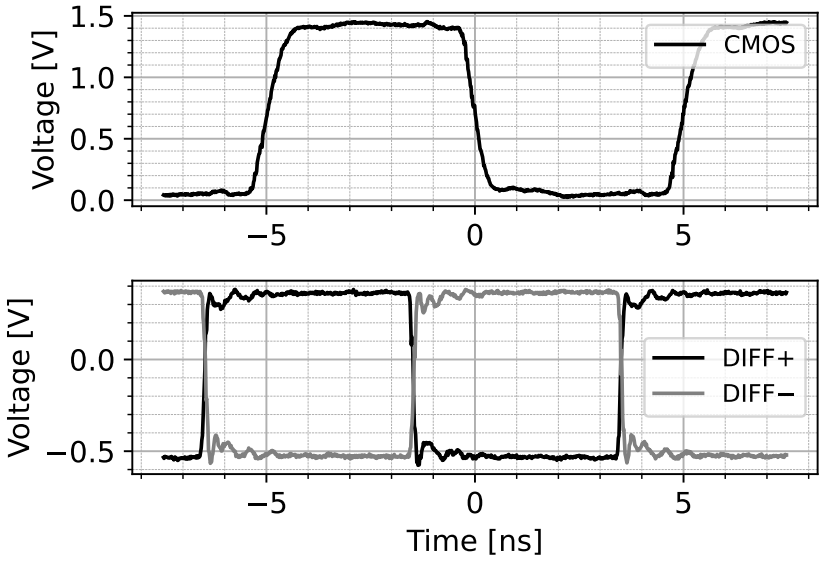


Figure 4: The trace shows a 100 MHz clock output. The 20% to 80% rise times are 75 ps and 0.6 ns, respectively, for the differential and CMOS outputs.

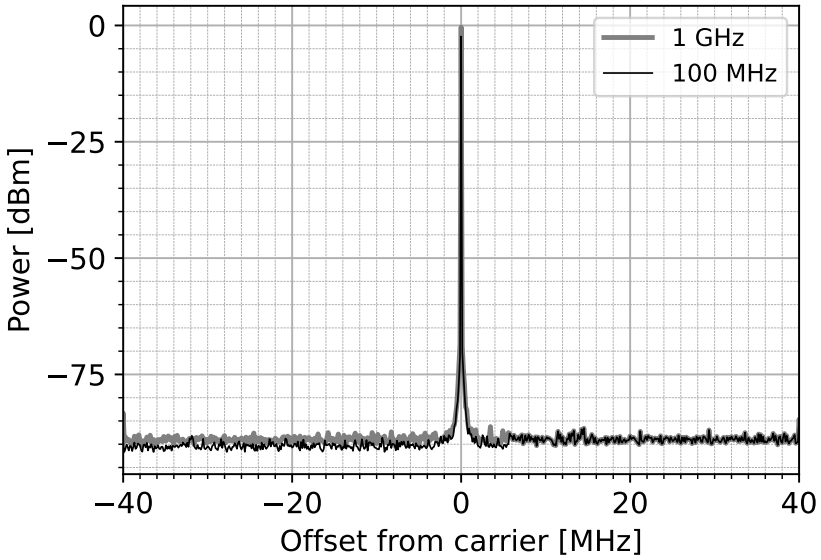


Figure 5: This high resolution scan shows a 80 MHz span around 100 MHz and 1 GHz clocks. Only two features are present: the clock itself and the spectrum analyzer's noise floor (around −85 dBc) everywhere else. The CG792's spur-free clock allows acquisition and reconstruction of waveforms with a high SFDR.

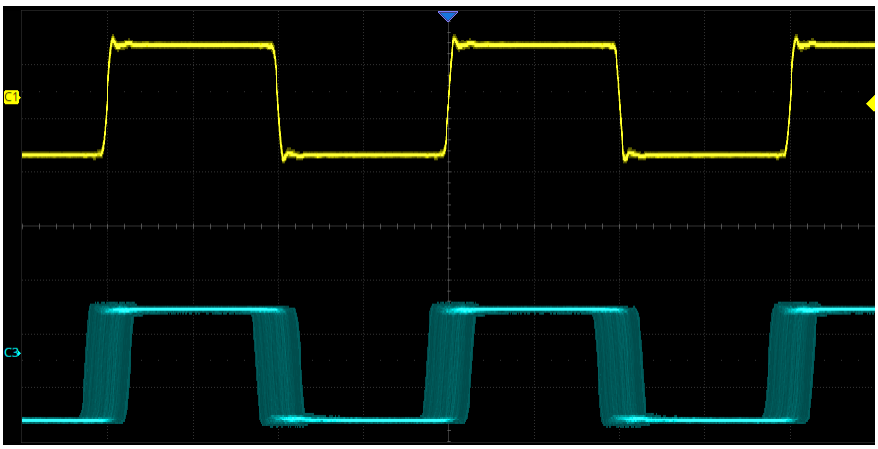


Figure 6: The CG792 allows the application of up to 3 ms of jitter to any of the output channels. The upper scope trace is a clean, unmodulated clock. The lower one is modulated with 5 ns of jitter. Traces shown at 500 mV/div, 10 ns/div, with infinite persistence.

1 Introduction

This chapter describes the basic functionality of the CG792 Multichannel Clock Synthesizer.

1.1 Feature Overview

The CG792 Multichannel Clock Synthesizer provides two channels of precise, low-jitter digital clock signals for applications ranging from the development of digital circuits to the testing of communications networks. The instrument can be extended by up to two additional output channels.

The CG792 generates single ended and differential clocks from 1 mHz to 2.2 GHz with sub-picosecond jitter. Clock frequencies may be set with up to 11 significant digits. Differential outputs have continuously adjustable offsets and amplitudes. Edge transition times are typically 80 ps. Several instrument features support more complex tasks. The phase of the outputs may be adjusted with 25 ps resolution at frequencies above 200 Hz, and 80 ns resolution below 200 Hz. The outputs can be modulated with internally generated waveforms, or using an external analog modulation input.

The standard crystal oscillator timebase of the CG792 provides sufficient accuracy for many applications. An optional ovenized crystal oscillator, or rubidium frequency standard, may be added to improve frequency stability and reduce aging. The CG792 may also be locked to an external 10 MHz timebase. The CG792 delivers a low spurious output signal. Phase noise for a 100 MHz carrier at 100 Hz offset is less than -100 dBc/Hz, and the spurious response is better than -70 dBc. All instrument functions may be controlled from the front panel or via the USB, Ethernet, or RS-232 interfaces. A universal input AC power supply allows world-wide operation.

1.2 Front Panel Overview

The front panel was designed to provide a simple, intuitive, user interface to all the CG792 features (see Figure 1.1). The CG792 can be controlled from the graphical user interface (GUI) displayed on the front-panel touchscreen. The GUI is organized around a set of tabs, providing easy access to all instrument functionality. See Section 1.4 on page 22 for more information on using the GUI.

1.2.1 Pushbuttons

The power switch is located in the lower right corner of the front panel. Pushing the switch enables power to the instrument. Pushing the switch again (and confirming on the GUI) places the instrument in stand-by mode, where power is enabled only to optionally installed timebases. Power to the main board is turned off in stand-by mode. Long press of the power button places the instrument in stand-by mode without GUI confirmation.

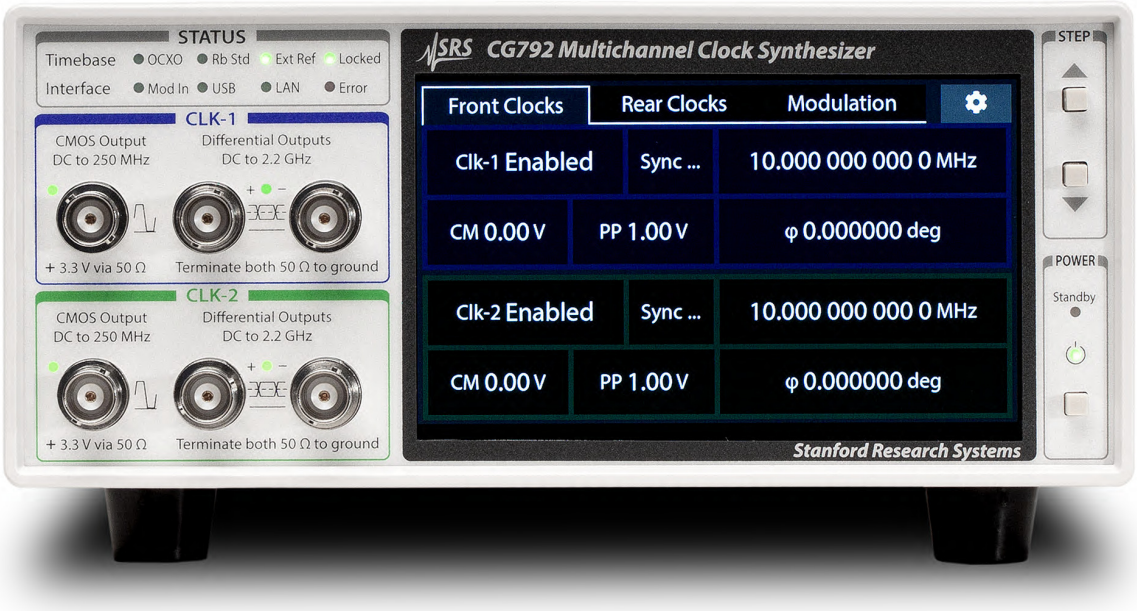


Figure 1.1: The CG792 Front Panel

Two 'Step' pushbuttons on right side of the panel above the power switch can be used to increment or decrement the currently selected digit/parameter, as indicated by the rectangular box drawn over the digit/parameter. A different digit or parameter may be selected by touching it on the screen.

1.2.2 BNC Outputs

The front panel provides two sets of three output drivers for connecting the CG792 clock signals to user applications via standard BNC cables. The leftmost connectors provide a CMOS output driver. The other outputs are complementary, high-speed output drivers.

1.2.3 Timebase and Interface Status Indicators

In the upper left portion of the front panel are two groups of LED indicators. The upper group is labeled "Timebase". The meaning of the indicators is as follows:

OCXO : The instrument uses the optional internal ovenized crystal oscillator frequency reference.

Rb Std : The instrument uses the optional internal rubidium frequency standard.

Ext Ref : The instrument has detected an external 10 MHz reference at the 10 MHz input BNC on the rear panel of the CG792. The CG792 will lock its internal clock to this external reference.

Locked : When lit, this LED indicates that the reference output has been stabilized and is locked to the provided optional timebase (OCXO or rubidium) or external reference.

The lower group of LED indicators is labeled "Interface". These LEDs indicate the current status of Ethernet (LAN) and USB remote programming interfaces. Each of these LEDs will briefly flash when the instrument accepts a command over the relevant interface. If a command received over the remote interface fails to execute due to either a parsing error or an execution error, the Error LED will illuminate and stay lit until the error queue is read out via the GUI or any remote interface. The 'Mod In' or 'Mod' LED is illuminated whenever modulation is not turned off.

1.3 Rear Panel Overview

The rear panel provides connectors for AC power, remote interfaces (Ethernet, USB, RS-232), external digital or analog modulation inputs, external reference input, two reference outputs, and optional clock outputs (see Figure 1.2).

1.3.1 AC Power

The Power Entry Module is used to connect the CG792 to a power source through the power cord provided with the instrument. The center pin is connected to the CG792 chassis so that the entire box is grounded.

The source voltage requirements are: 90 to 132 VAC or 175 to 264 VAC, 47 to 63 Hz (125 VA total).

Connect the CG792 to a properly grounded outlet. Consult an electrician if necessary.

1.3.2 Ethernet, USB, RS-232

The CG792 comes standard with communications ports for Ethernet, USB, and RS-232 operation. A host computer interfaced to the CG792 can perform any operation that is accessible from the front panel. Programming the CG792 is discussed in the CG792 Remote Programming chapter on page 47.

The Ethernet uses a standard RJ-45 connector to connect to a local area network (LAN) using standard Category-5 or Category-6 cable.

Figure 1.2: The CG792 Rear Panel

The USB interface uses a Type B connector and is implemented as a serial port emulator. The communication parameters are: 115200 Baud, 8 Data bits, 1 Stop bit, No Parity, no Flow Control. The baud rate is fixed.

The RS-232 interface connector is a standard 9 pin, type D, female connector configured as a DCE (transmit on pin 2, receive on pin 3). The default communication parameters are: 9600 Baud, 8 Data bits, 1 Stop bit, No Parity, no Flow Control. The baud rate can be changed using the GUI or via a remote command.

1.3.3 External Modulation

The rear panel provides two external modulation inputs. The digital modulation input accepts a signal with a nominal 3.3 V high level relative to ground. The signal passes through a high-speed comparator and then distributed to the clock channel outputs. The digital modulation can be applied in several ways: as clock channel blanking or inversion control, or to control modulation on/off.

The analog modulation input is digitized by a 14-bit, 1 MSPS ADC. The modulation data can be applied as frequency or phase modulation with an adjustable modulation depth and sampling rate. The Output Modu-

lation section on page 37 provides further information about the use of analog modulation.

1.3.4 10 MHz In / Outputs

The CG792 provides a 10 MHz BNC input for synchronizing its internal clock to an external 10 MHz reference. The external reference should provide greater than 1 V_{pp} into a 50 Ω impedance. The CG792 will automatically detect the presence of an external 10 MHz reference and lock to it if possible. If the CG792 is able to lock to the external reference, the front-panel Ext Ref LED will turn on and stay on until the reference is removed.

The CG792 provides two 10 MHz BNC outputs for synchronizing other instrumentation to the CG792's timebase. These two outputs are independently transformer-coupled to the internal frequency synthesis circuit.

1.3.5 Clock Output Options

Up to two additional output channels can be installed in the CG792. As with the two standard channels, the optional channels provide single-ended and differential clock outputs with identical specification. The connectors for the additional outputs are available on the right side of the rear panel. The control of all outputs is through the front-panel touchscreen or remote interfaces.

1.4 Navigating the GUI

A touch screen, color LCD display provides easy access to status and configuration information for the CG792. All settings of the CG792 may be easily updated through interaction with the display. The following paragraphs are meant to guide the user in interacting with the graphical user interface.

The interface is organized into three tabs, with an additional settings menu. To switch between the tabs, touch the buttons on the top line of the display.

1.4.1 Clocks Tab

The first two tabs (Fig. 1.3) provides an overview of the state of the clock output channels. The front two outputs are shown on the first tab, and the optional rear channels on the second tab, if installed.

Parameter adjustment is simple. First, touch the parameter that needs to be changed. A keypad or menu will appear. In the menu, select the desired option, or touch the cross button to close the menu.

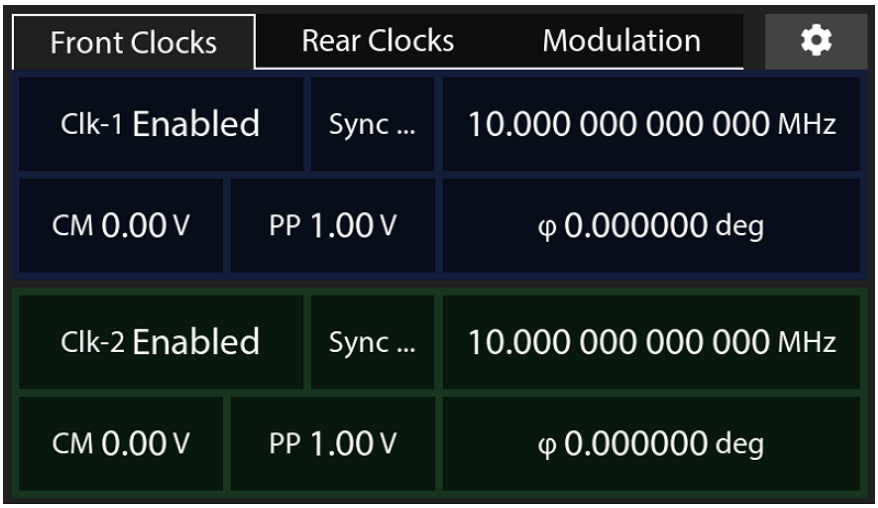


Figure 1.3: Clocks Tab

In the keypad (Fig. 1.4), type in the new value and conclude entry by touching a unit key, if displayed, or the enter key. In the latter case, the number will assume the units that were in use before numeric entry was initiated.

To change the step size used by the 'Step' pushbuttons, touch on one of the digits in the parameter value currently displayed in the keypad window. Alternatively, touch 'Step ...' and directly enter the desired step size.

Each of the outputs can be synchronized to one of two other channels by means of the 'Sync ...' menu. Click on the 'Sync ...' button, and select which clock to synchronize to.

Figure 1.4: Keypad

1.4.2 Modulation Tab

The 'Modulation' tab (Fig. 1.5) allows the user to modulate the clock outputs in several different ways. Depending on the modulation mode and type selected, the available parameters can be different than those shown in the figure. For details, consult the Operation chapter (section Output Modulation on page 37).

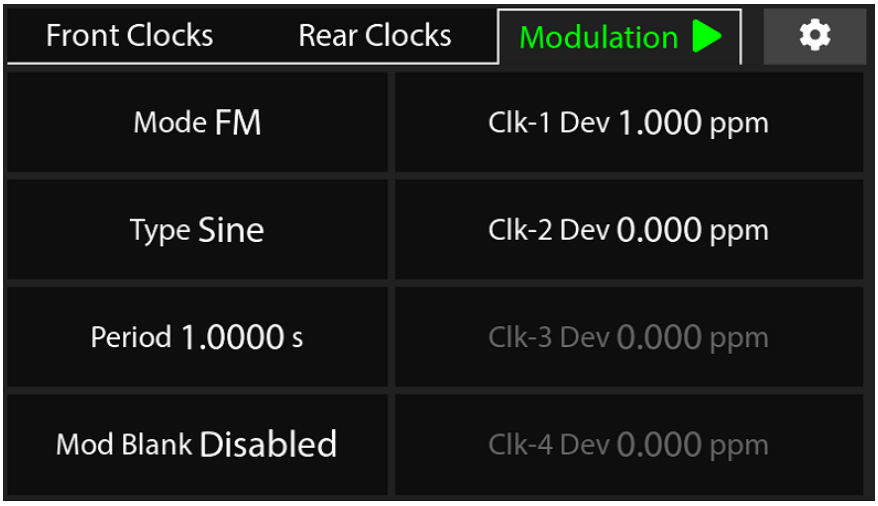


Figure 1.5: Modulation Tab

1.4.3 Settings

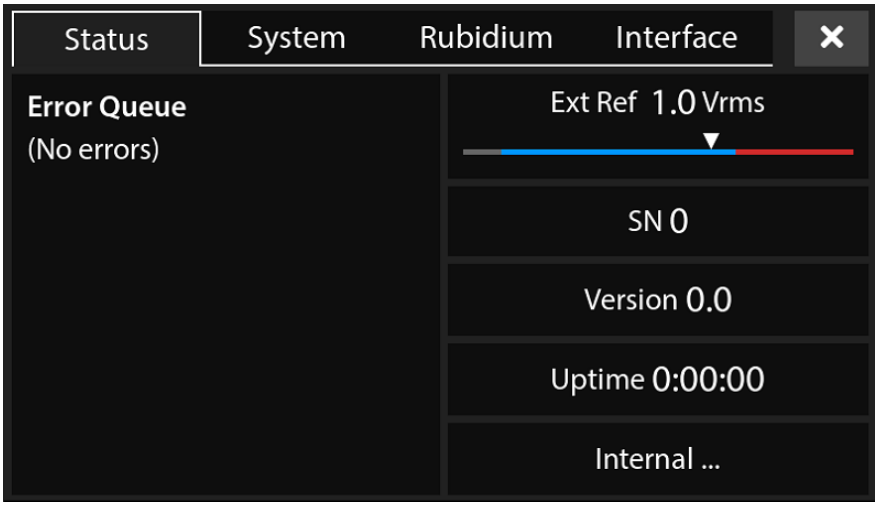


Figure 1.6: Settings window

The 'Settings' window (Fig. 1.6) is accessed by touching the "gear" icon at the top right corner of the main screen. The window is organized in a similar fashion as the main screen. There are three or four tabs, depending on the selected optional timebase, which allow the configuration of

system parameters and monitoring of the operational parameters. See Section 2.7 for more details about the available settings.

1.5 Getting Started

This section presents several example tasks to help you become familiar with the basic and advanced operation of the CG792 Multichannel Clock Synthesizer. Each example can be completed from the front-panel GUI without any external computer control.

The following equipment is needed to complete the tutorials in this section:

- CG792with the included power cord
- Two- or four-channel oscilloscope
- Several 50 Ω BNC cables, ideally all of identical length, type, and manufacturer
- 50 Ω terminators
- 50 Ω feed-through terminator (unless the oscilloscope has internal termination)

1.5.1 Example 1: Generating a Simple Clock Signal

This exercise demonstrates how to generate a single frequency clock and verify it on an oscilloscope.

1. **Connect the Instrument.** Connect the CG792 to AC power and press the power button in the lower-right corner of the front panel. Wait until the startup sequence and internal self-tests complete, then put the instrument into a known starting configuration:
   (a) Touch the 'gear' icon at the top right (⚙)
   (b) Touch the 'System' tab at the top
   (c) Touch the 'Recall …' tile
   (d) Touch the 'Factory Defaults' tile (lower right)
   (e) Touch the × at the top-right of the screen to exit the Settings window
2. **Disable the Output.** On the *Clocks* tab, locate Clk-1. In the default configuration, the state is shown as 'Enabled'. Touch the field and select 'Disabled'.

3. **Connect the Output.** Using a 50 Ω BNC cable, connect the DIFF+ BNC output of Clk-1 (top middle BNC on the front panel) to an oscilloscope channel. If your oscilloscope input is set to high-impedance input, use a 50 Ω feed-through terminator at the oscilloscope input for best signal quality. Terminate the other differential output (DIFF−) with a 50 Ω termination.
4. **Enable the Output.** On the *Clocks* tab, locate Clk-1. The state should be shown as 'Disabled'; touch the field and select 'Enabled'. Observe the clock signal on the oscilloscope.
5. **Set the Frequency.** By default, the frequency is set to 10 MHz. Touch the frequency display for Clk-1, enter 25 and touch the 'MHz' key. The output frequency should now be 25 MHz.
6. **Adjust the Amplitude.** Touch the field that displays the peak-to-peak voltage in units, displayed in the format 'PP 1.00 V' and enter a new amplitude, such as 0.5 V. Verify that the oscilloscope displays a 25 MHz square wave of the desired amplitude.
7. **Change Step size.** Touch the amplitude tile again so that the keypad is displayed. In the large numeric display, press the digit '5'; this sets the step size to 100 mV. Press the up and down pushbuttons to adjust the amplitude to 0.3 V. Then touch the 'Step …' tile above the numeric display and enter 0.25 V. Use the up and down buttons again to observe the effect of the new step size.

This completes the most common use case: generating a stable, low-jitter clock output from the CG792.

1.5.2 Example 2: Synchronizing Two Channels

This example shows how to generate two synchronized clock outputs and verify their relative phase.

1. Perform instrument startup and reset as shown in step 1. of Example 1.
2. Connect the DIFF+ Clk-1 and Clk-2 to two channels of an oscilloscope, both terminated in 50 Ω.
3. On the *Clocks* tab, enable both channels.
4. Set both frequencies to 100 MHz. The two signals will now run independently but at the same nominal frequency. The phase difference between the two channels should remain constant on the scope.
5. Touch the 'Sync …' button for Clk-2 and select Clk-1. After a short

delay, the front-panel display will report synchronization complete.

6. Observe the oscilloscope traces. The two outputs should now rise simultaneously within a few tens of picoseconds, limited by cable delay. If the delay is significantly larger, make sure to check that the two cables are not only the same length, but also the same type as indicated on the markings on the cable. Different dielectrics can make for significantly different electrical lengths.
7. Now set the two clocks to different frequencies: set Clk-1 to 25 MHz and Clk-2 to 50 MHz. Try two different sync routes:
   (a) Press the upper 'Sync …' button (in the Clk-1 region), and select 'Clk-2'. Observe that both outputs have now been set to 50 MHz, and have zero phase with respect to each other.
   (b) Again set Clk-1 to 25 MHz and Clk-2 to 50 MHz.
   (c) Press the *lower* 'Sync …' button (in the Clk-2 region), and select 'Clk-1'. Check that the outputs are now in sync at 25 MHz.

1.5.3 Example 3: Applying Frequency Modulation

This final example introduces internal frequency modulation (FM) using the *Modulation* tab.

1. Perform instrument startup and reset as shown in step 1. of Example 1.
2. Set both Clk-1 and Clk-2 active at 10 MHz. Trigger the oscilloscope on Channel 1 (Clk-1). Observe the two channels on an oscilloscope, making sure the full period of each fits on the screen.
3. Navigate to the 'Modulation' tab. Touch the 'Mode' field and select 'FM' from the menu that appears. Then touch 'Type' and select 'Sine'. Finally, enter 1 s for the Period.
4. Touch the deviation field (top right of the screen) for Clk-2 and enter 0.01 ppm. The phase between the two channels, as seen on the oscilloscope screen, will now oscillate with a period of one second due to the selected frequency modulation.
5. Select 'Mode' and touch 'Off' to return to a fixed-frequency output. When the mode change is in progress, the clock output may disappear for a moment while the circuitry is reconfigured.

These examples illustrate the fundamental operations—enabling outputs, synchronizing channels, and adding modulation—that form the basis of more complex CG792 applications.

2 Operation

This chapter provides an in-depth look at operation of the CG792 Multichannel Clock Synthesizer.

2.1 Instrument Power On and Off

At power on, the CG792 performs a number of self tests to verify that it is operating correctly. If any of the tests fail, the CG792 will briefly display a warning after the test. In such a case, contact SRS or an authorized representative to repair the unit. After the self tests have completed, the CG792 will recall the latest known instrument settings from nonvolatile memory and be ready for use.

The instrument is normally powered off by a short press of the power button (front panel, lower right). The GUI will display a menu asking for confirmation. If the powerdown is confirmed, the current settings will be saved in memory location 0.

To prevent the nonvolatile memory from wearing out, the CG792 will not automatically save instrument settings except when powerdown is confirmed on the GUI, and when explicitly saving parameters via the front panel or the remote command `*SAV`. Saved settings can be recalled using the `*RCL` remote command. See the CG792 Remote Programming chapter for more information about these commands.

The CG792 can be forced to recall the factory default settings. This is accomplished by recalling the memory location 8 via the front panel or remote command. (There is no separate "power-on factory reset" functionality.)

The instrument can also be powered down by long-pressing the power button until the unit turns off. In that case, the settings will not be saved. Turning the CG792 off in this manner is not recommended since the abrupt loss of power may damage the output drivers.

2.2 Clock Outputs

The CG792 provides multiple types of clock outputs to suit different applications. High-speed differential outputs deliver precise complementary signals with adjustable amplitude and offset, while the CMOS output provides a single-ended digital signal with standard logic levels. The following subsections describe the characteristics and user-adjustable parameters of each output type.

2.2.1 Differential Outputs

The + and − outputs on the front panel are high-speed, differential drivers that operate with a nominal 50 % duty cycle. The rise and fall times of these outputs are <100 ps. The outputs provide fast, complementary voltages at the selected frequency, amplitude, and offset. To operate at specification, both outputs should be terminated into 50 Ω, even if only one output is used.

The user has the ability to adjust the common-mode voltage and peak-to-peak amplitude of the differential outputs in the range given in the Specifications table on page 3.

2.2.2 CMOS Output

The CMOS output provides 0 V and 3.3 V levels at a 50 % duty cycle. The transition times of this output are less than 1.0 ns (10% to 90%). It drives the output for frequencies ranging from DC to 250 MHz. At frequencies above 250 MHz, the CMOS driver will be turned off and forced to zero volts.

Despite its relatively high speed, the CMOS output does not need to be terminated with a 50 Ω load. Terminating the output will not harm the instrument but it will divide the output voltage levels in half. The CMOS output has a 50 Ω source impedance and so will reverse terminate pulses which are reflected back from the user's (unterminated) target system. Nevertheless, somewhat cleaner square waves with reduced rise times and reduced reflections can be obtained using the termination, keeping in mind that the voltage will be divided by two.

The CMOS output amplitude and common-mode voltages are fixed (see Specifications table on page 4).

2.3 Manipulating Parameters

The CG792 provides several numeric parameters for each output channel that can be monitored and adjusted via the front panel. These parameters include frequency, phase, common-mode voltage, and peak-to-peak voltage. The following subsections describe how to display, modify, step, and change the units of these parameters, giving the user precise control over the output signals.

2.3.1 Displaying a Parameter

The CG792 has four numeric parameters for each of the output channels: frequency, phase, common-mode voltage, and peak-to-peak voltage. (The last two, the common-mode and peak-to-peak voltages, apply exclusively to the differential outputs.) These parameters are displayed on the first two tabs of the front panel.

If a clock voltage or frequency parameter has more digits than fit in the provided button on the display, the value will be truncated with '…'. In that case, touching the parameter will display the full value together with the keypad that can be used to change units such that the value display requires fewer digits and thus is not truncated.

2.3.2 Changing a Parameter

To change a parameter, touch it and enter a new value using the numeric keys in the keypad, and complete the entry by touching the appropriate units key, or touching the enter key ( ). If the user enters extra digits beyond the allowed resolution of a parameter, the extra digits will be ignored.

2.3.3 Stepping a Parameter

Most of the numeric parameters can be stepped up and down by exact factors of ten by touching the 'Step' pushbuttons to the right of the display. To select the desired power of ten, touch the appropriate digit on the large numeric display in the keypad. A white rectangular frame surrounding the digit provides a visual cue to inform the user of the digit that will change when the parameter is stepped up or down. Alternatively, touch 'Step ...' and directly enter the desired step size.

Parameters that take a menu selection rather than a numeric value can usually be stepped through the available menu selections. The Clock Mode parameter is the exception: stepping only switches between the Low/High and Off/On pairs. See Section 2.4.1 for more details.

2.3.4 Changing Units

Frequency has the option of being displayed in units of GHz, MHz, kHz, Hz, or mHz. When the user enters a frequency using the front panel, the CG792 will display the frequency in the units used to complete the entry. For example, touching the keys '1', '0', 'kHz' sequentially, to change the frequency to 10 kHz, will cause the CG792 to display the result in the units of kilohertz. The user can change the displayed units by touching a different units key. The same principle applies to other dimensional parameters.

2.4 Clock Parameters

Each clock output channel on the CG792 has a set of parameters that control its behavior, waveform characteristics, and signal levels. These parameters include output mode, frequency, phase, and voltage levels. The user can view and adjust them via the front-panel interface or remotely using the corresponding commands. The following subsections describe each parameter in detail.

2.4.1 Mode

For each clock channel, the following modes can be selected from the front-panel menu, or the corresponding remote command `SOUR#:STAT`:

- **Disabled.** The clock output is set to output a constant zero volts on both the differential and CMOS outputs.
- **Enabled.** Clock is configured for normal operation, with frequency and voltage as selected by the clock parameters.
- **Ext Invert.** Differential outputs have their polarity inverted whenever the external digital modulation input is asserted (that is, when 3.3 V is applied to it). Note that the CMOS output is not affected.
- **Ext Blank.** Both the differential and CMOS outputs will be blanked whenever the external digital modulation input is asserted. The blanking level (either LOW or HIGH) can be selected from the Settings menu. See Section 2.4.2 for more details.
- **PRBS.** Instead of outputting a steady clock signal, the clock channel will output a PRBS-31 sequence (see Section 2.4.3) when this option is selected.
- **Low.** Hold the output blanked at a LOW level. Frequency parameter is grayed out and not adjustable from the GUI when clock is held Low.
- **High.** Hold the output blanked at a HIGH level. Frequency parameter is grayed out and not adjustable from the GUI when clock is held High.

The Mode parameter is unique with regard to its behavior using the Step up/down front-panel pushbuttons. Instead of stepping through all the available options as per the above list, the effect of stepping is as per Table 2.1.

Current Mode	Step	Result
Disabled	↑	Enabled
Ext Invert	↑	Ext Blank
Low	↑	High
Enabled	↓	Disabled
Ext Blank	↓	Ext Invert
High	↓	Low
(Else)	↑ / ↓	*(No change)*

Table 2.1: Stepping behavior for Clock Mode.

2.4.2 External Blanking

Blanking is used to temporarily suppress (turn off) the signal outputs without stopping or reconfiguring the signal source itself. When blanking is active, both the differential and CMOS outputs are forced to their blanked state, preventing any valid output signal from being delivered to downstream circuitry. The blanked state can be either low or high, depending on blanking polarity—see Section 2.7.2 for more details about Blank Pol.

This is typically used to:

- Prevent unwanted output during setup or reconfiguration,
- Gate the output in synchronization with external events, or
- Protect downstream equipment during transitions or measurement dead time.

2.4.2.1 How to Activate Blanking

External blanking is controlled by the external digital modulation input, together with a per-clock-channel enable.

First, enable blanking by touching the appropriate clock state parameter. For example, if Clk-1 is currently enabled, touch the field that says 'Clk-1 Enabled.' From the menu that appears, select 'Ext Blank'.

When the clock enable parameter shows 'Clk-1 Ext Blank' (and similarly for other clocks), the blanking is enabled. Thus, when the external digital modulation input is asserted (high), the outputs are blanked. When the external digital modulation input is de-asserted (low), normal signal output resumes. Blanking takes effect immediately upon the input changing to the asserted level.

2.4.2.2 Physical Connections

To use external blanking:

- Ensure the digital control signal (from a microcontroller, FPGA, logic output, or similar source) meets the specified logic-level requirements for the input: 0 V (low) and 3.3 V (high).
- Connect the signal to the external digital modulation input on the instrument rear panel.
- Connect the CG792's signal outputs (differential and/or CMOS) to the downstream equipment as usual.

No additional wiring is required beyond the blanking control signal.

2.4.2.3 Runt Pulses

The internal blanking switch may produce very short, nanosecond-scale transitions—commonly referred to as runt pulses—during the changeover between the blanked and active states.

These transients are extremely brief and generally do not affect normal operation. However, they may momentarily appear on the differential or CMOS outputs during blanking transitions.

To prevent unintended effects on sensitive downstream equipment, select one of these options:

1. Use blanking only when the connected circuitry can tolerate brief, narrow pulses. Avoid switching blanking during critical measurement intervals. Or:
2. Make sure that the blanking control signal applied to the digital modulation input is of the same frequency as the blanked clock output. Additionally, the blanking must be asserted during the half of the clock cycle opposite to the Blank Pol setting:
    - If Blank Pol is set to Low, blanking should be asserted (and/or deasserted) when the clock output is high.
    - If Blank Pol is set to High, blanking should be asserted (and/or deasserted) when the clock output is low.

By following these guidelines, external blanking can be used safely and effectively without disturbing connected equipment.

2.4.3 PRBS

PRBS-31 (Pseudorandom Binary Sequence of length $2^{31}-1$) is a long, deterministic bit pattern that mimics random data for testing high-speed digital links and signal integrity. It is generated using a 31-bit linear feedback shift register (LFSR) and repeats only after 2,147,483,647 bits, providing excellent coverage of possible bit transitions. Because its spectral and statistical properties resemble white noise, PRBS-31 is widely used to stress-test serializers, receivers, and transmission paths for bit errors and jitter performance.

On the CG792 the PRBS output is available from any of the clock outputs, both CMOS and differential, up to 100 MHz, so long as modulation is not enabled on the same clock channel at the same time. Each clock channel runs an independent PRBS-31 generator.

The “symbol” values update at the programmed clock frequency. For example, when running at 100 MHz PRBS, the shortest low (or high) pulse will be 10 ns. In contrast, when the clock is simply enabled for

normal operation at 100 MHz, each pulse will be low for 5 ns and high for 5 ns.

Phase adjust is disallowed during PRBS operation.

2.4.4 Frequency

The CG792 can output frequencies in the range 1 mHz to 2.2 GHz with up to 11 significant digits. The frequency may be set to arbitrary values, or stepped up and down by following the instructions described in the Stepping a Parameter section at the beginning of this chapter (page 32). All significant digits can be entered via the front panel. If the user enters more than the available number of digits, the result will be truncated. If the user enters an invalid frequency, the CG792 will display an error message and leave the frequency unchanged.

The CG792 truncates both the frequency and the frequency step size to the available resolution when the frequency changes. Normally, when the user steps the frequency up and down by a small amount, the CG792 will seamlessly slew the output to the new frequency. If the user crosses an octave boundary, however, the CG792 will adjust to the new frequency by recalibrating its internal PLL, which can break phase continuity. The octave boundaries are a consequence of the CG792 generating all output frequencies by dividing down the output of an RF VCO that operates from 3.2 GHz to 6.4 GHz, which is a little more than one octave of tuning range.

2.4.5 Phase

The phase may be set to arbitrary values, or stepped up and down by following the instructions described at the beginning of this chapter. Phase adjustment is available when a clock channel is not disabled or blanked, modulated, or outputting PRBS.

The CG792 will integrate phase steps in the main display until the phase reaches $\pm 720°$, at which point it will wrap the phase back to $-720°$. This is accomplished by adding or subtracting 720° from the value to make it fit in the range $\pm 720°$. For example, if the current phase is 700° and the user steps the phase 90°(e.g. by touching the '+90°' button on the 'Sync' tab), the CG792 will display 70°.

Internally, the CG792 will first subtract multiples of 360 degrees, then subtract 180 degrees and invert clock polarity, if appropriate. The remaining phase shift is executed as a combination of frequency detuning and clock divider adjustment.

When the user changes frequency, the CG792 will automatically reset the phase display to 0°. Nevertheless, small frequency adjustments gen-

erally do not change the phase abruptly, except when that is unavoidable (e.g., at the end of the VCO tuning range).

The phase is displayed with the number of decimal places limited in accordance with the resolution specified on page 3.

2.4.6 Levels and Amplitude

The user can adjust the common-mode voltage ('Vcm') and peak-to-peak voltage ('Vpp') of the differential outputs. The levels of the CMOS output are fixed as 0 V and +3.3 V nominal.

To enter the voltages, use the keypad and complete the numeric entry using the appropriate units.

2.5 Phase Synchronization

When a definite phase relationship is desired between two or more channels, the phase synchronization feature is available. The synchronization works by frequency-detuning one of the pair of channels until they are in a zero-phase relationship to each other. Following the sync event, the clocks can be adjusted independently of each other. Of course, if the frequency is changed, the relative phase between the channel will drift according to the magnitude and duration of the detuning.

As represented in Fig. 2.1, only certain pairs of channels can be directly synchronized with each other. For example, if it is desired to sync Clk-1 to Clk-4, first Clk-1 has to be sync'd to Clk-2, and then Clk-2 needs to be sync'd to Clk-4. (Alternatively, this can also be done via Clk-3 instead of Clk-2.)

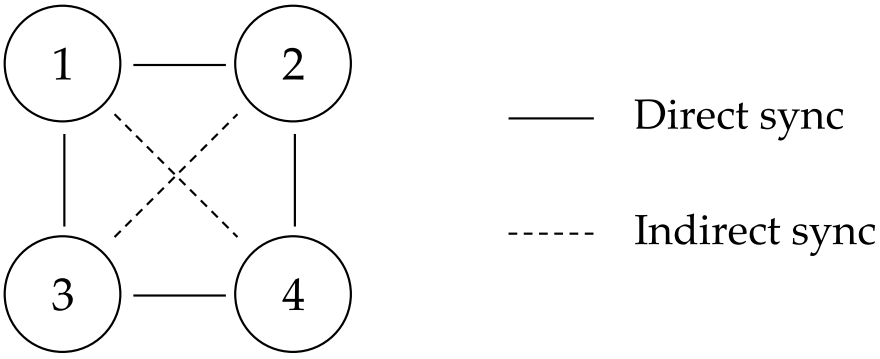


Figure 2.1: Possible channel synchronization synchronizations.

2.6 Output Modulation

The CG792 presents the user with several ways to modulate the clock output frequency and phase. Regardless of the modulation options,

the outputs remain square waves. The CG792 does not have amplitude modulation capability.

The modulation can be controlled either via the GUI 'Modulation' tab or the remote commands. Both differential and CMOS outputs are equally affected by the modulation.

2.6.1 Modulation Mode

There are four modulation modes available. To select between them, use the 'Mode' parameter on the 'Modulation' tab on the front panel, or send a `MOD:MODE` remote command. The selected modulation mode applies to all installed channels simultaneously.

When modulation mode is set to Off, the modulation of all clock channels is disabled. The output is a fixed-frequency, fixed-phase clock signal according to the settings of each individual channel.

2.6.2 FM

When frequency modulation (FM) is selected as the Modulation Mode, the nature of the modulation depends on the *Modulation Type* selected. There are five types available: Sine, Triangle, Square, Noise, External.

For the internally generated waveforms (Sine, Triangle, and Square), the period of the waveform can be set using the 'Period' button on the 'Modulation' tab, or the corresponding remote command, `MOD:PERiod`. The modulation period adjustment applies to all modulated channels equally.

For noise and external analog frequency modulation, the modulation sample rate is adjustable instead of the modulation period. This sample rate represents the rate at which frequency changes are applied. For external analog FM, the highest frequency component of the sampled analog voltage needs to be less than half of the selected sample rate according the usual Nyquist relations. For noise, the sample rate affects the spectral shape of the modulated clock as well as the maximum expected phase drift resulting from the modulation.

For frequency modulation, the modulation deviation can be individually adjusted for each channel. The adjustment is entered in parts per million, referring to the carrier frequency. For example, if Clk-1 is set to output a 10 MHz carrier, and a 1 ppm modulation deviation is entered, then the output frequency will oscillate between positive and negative 10 Hz away from 10 MHz.

For external analog modulation, the unit for deviation is ppm/V, which provides the scale factor for converting the external analog input to frequency deviation (in ppm).

2.6.3 External Phase Modulation (Ext PM)

The external analog modulation input can be used to apply a phase modulation (PM) to the output signal. In this case, the modulation is expressed as a time delay of the clock edges, proportional to the applied input voltage.

The effect of this modulation depends on the *modulation sample rate*, f_s, which is the rate at which the modulation samples are applied to update the clock phase. If V_{in} is the applied voltage and K_{PM} is the modulation sensitivity (in μs per volt), then the maximum phase shift per sample is

$$\Delta t_{max} = \frac{K_{PM} \cdot V_{in}}{2f_s}.$$

In practice, this means that increasing the modulation sample rate reduces the instantaneous time shift for the same input voltage, limiting the effective range of clock deviation. Conversely, a lower sample rate increases the time shift per voltage, allowing a larger phase excursion.

2.6.4 Jitter

In jitter mode, the clock edge of the modulation clock is randomly modulated. All modulated channels share the same peak-to-peak deviation; however, the modulation can be individually enabled or disabled for each channel separately.

When jitter is active, the sample rate is not user-adjustable. Instead, the modulation samples are delivered at the rate needed to result in the desired peak-to-peak modulation amplitude.

2.7 Settings

The 'Settings' window (Fig. 1.6) is accessed by touching the "gear" icon at the top right corner of the main screen. It provides information and controls for the remote interface and timebase configuration, display options, preset recall, and other parameters. The settings window is divided into four tabs as explained below. Note that the Timebase tab may not be present if no optional timebases are installed.

2.7.1 Status

The Status tab (see Fig. 2.2) is vertically divided into two halves.

On the left, there is a large box displaying instrument errors. If any error conditions occur, such as parameter over-range, they will be reported there and the 'Error' LED will illuminate on the front panel. Touching the error box will clear the errors and turn off the LED.

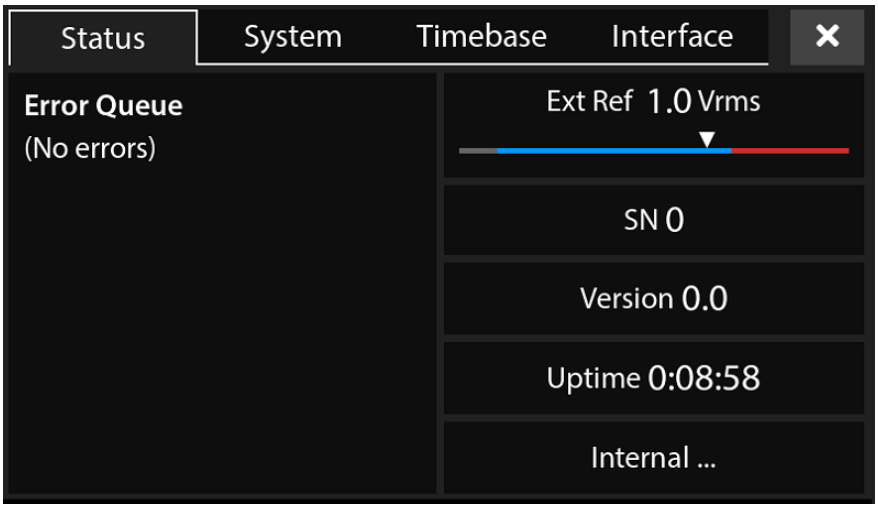


Figure 2.2: Settings: Status Tab

The right side of the Status tab provides additional information:

- **Ext Ref.** The indicator and number displayed give an approximate indication for the magnitude of the external 10 MHz reference, if any, that is supplied to the rear-panel BNC input. If using the external reference, aim to keep its magnitude in the central blue range of the indicator.
- **SN.** The number is the serial number of the instrument. When communicating with SRS regarding instrument calibration and/or repair, mention the serial number together with the model number (CG792) and the firmware version (next line).
- **Version.** This is the firmware version of the instrument.
- **Uptime.** Indicates how long the instrument has been powered on.
- **Internal ...** Touching this button opens a new window with several internal voltages and temperatures. Under normal operation, all values will be in their central green ranges. There is no need to monitor this information regularly.

2.7.2 System

The System tab (Fig. 2.3) allows control of the display backlight, blanking polarity, and saving/recalling instrument parameters. The left side of the parameters are as follows:

- **Brightness** can be set in percentage units to make the display brighter or dimmer. By default, the CG792 ships with brightness in the middle of the range.

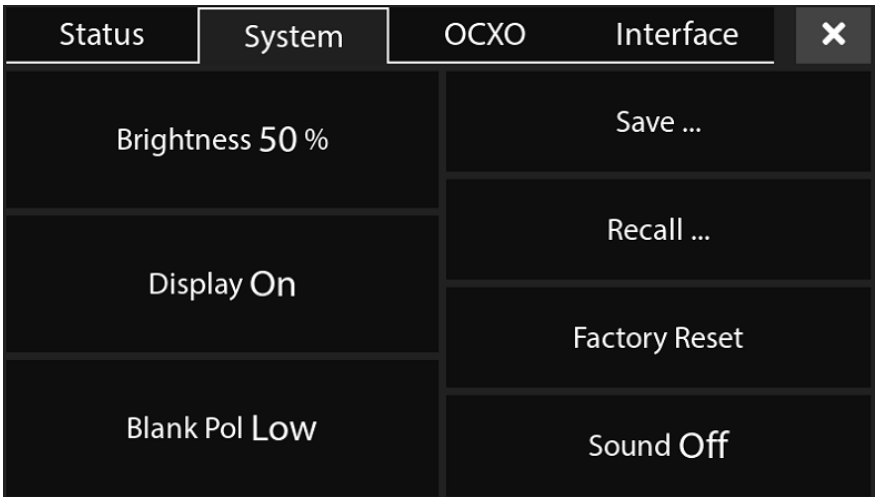


Figure 2.3: System Settings

- **Display** controls the time until the display backlight is turned off. By default, the display backlight will stay on perpetually; Touching this button opens a menu to configure an optional timeout.
- **Blank Pol** adjusts the blanking output polarity. When the mode of any of the clocks is set to 'Ext Blank', the clock will be blanked whenever the digital modulation input (rear-panel BNC) is asserted by a HIGH logic level (3.3 V). The blanking can force the clock in the HIGH or LOW states, as set by the 'Blank Pol' parameter.

  Note that when a clock mode is set to 'Low' or 'High', setting the 'Blank Pol' parameter will also affect the blanked clock. For example, even if the clock is set to 'Low', setting 'Blank Pol' to HIGH may force the clock output to a high level.

The parameters on the right side of the screen relate to saving and recalling the instrument configuration.

- **Save ...** is used to save the current configuration to one of seven memory locations. The button opens a menu where these locations are displayed as 1 through 7.

  The use of the 'Save ...' menu is equivalent to the `*SAV` remote command (page 63) with arguments ranging from 1 to 7 inclusive.

  When confirming powerdown, the current instrument configuration is written to the location 0. This allows the firmware to boot the instrument with the same values as were in effect before the powerdown.

  Note that the `SYSTEM:REBoot` (page 64) command does *not* save the

system settings. If a reboot is desired with settings saved, make sure to issue a `*SAV 0` before the reboot.

- **Recall ...** has the opposite effect of save, in that it recalls the parameters previously stored to the memory location. The menu has one additional button labelled 'Reset'. Touching it sets all non-communication parameters to their factory-default values.

  The 'Recall ...' menu corresponds to the `*RCL` remote command (page 62). The 'Reset' button is equivalent to restoring from memory location 8, that is, `*RCL 8`, or, equivalently, `*RST` (page 62).

  The three communication parameters (RS-232 baud rate, DHCP on/off, IP address) are always restored from memory location 0. In order to keep these parameters at the value in effect before recall, the Recall function first stores the current configuration to memory location 0, then restores non-communication parameters from the requested memory location, and finally restores the communication parameters from location 0.

- **Factory Reset** button prompts for confirmation and if confirmed, resets the instrument to the factory default configuration. All stored information and memory locations, including communication parameters, are cleared and set to the factory defaults.

- **Sound** menu allows choosing the button-press sounds between Off, Low, and High volume.

2.7.3 Timebase

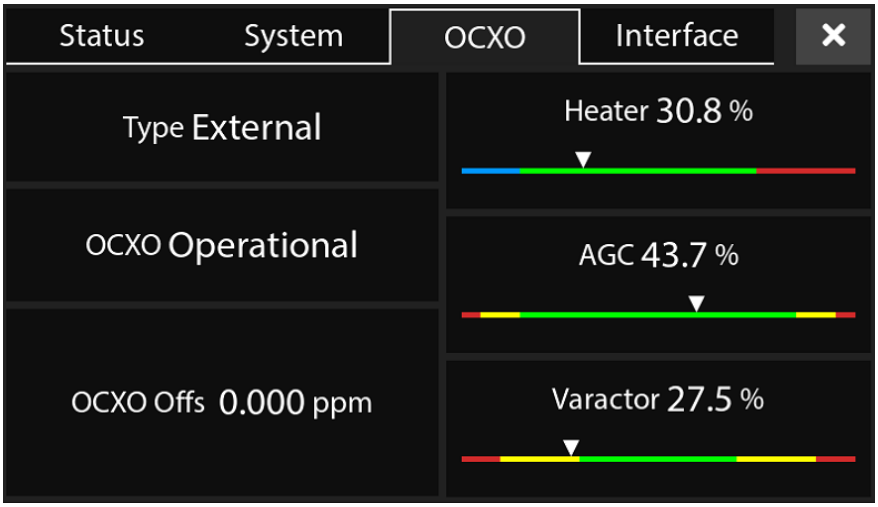


Figure 2.4: Timebase Settings

The OCXO tab (Fig. 2.4) is present whenever the OCXO optional timebase is installed in the instrument.

The only adjustable parameter is 'OCXO Offs', which can be used to detune the system timebase from its factory default value.

The other parameters are provided for monitoring the OCXO timebase status:

- **Type** shows whether the currently active timebase is the internal (OCXO) or the externally provided 10 MHz.
- **OCXO** shows the status of the OCXO. In normal operation, it states 'Operational'.
- **Heater** shows the current power level of the crystal oven heater. During warm-up, the heater power will display a large value, which settles down into the normal operating range within a few minutes.
- **AGC** refers to the Automatic Gain Control of the OCXO timebase. It is automatically adjusted to maintain stable operation of the timebase.
- **Varactor** is tuned to allow for frequency control. The control can be done using the 'OCXO Offs' parameter, and the Varactor level can be used as confirmation that the change has been registered.

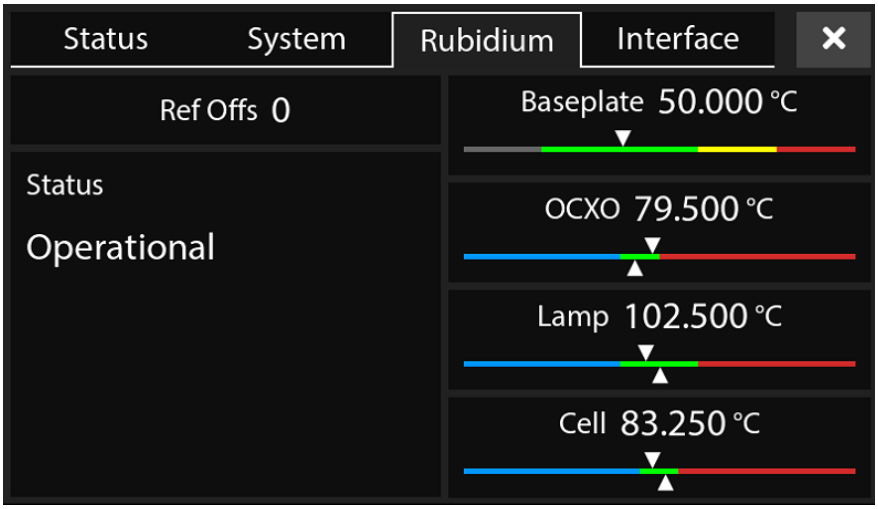


Figure 2.5: Timebase Settings (Rb reference)

If the optional rubidium timebase is installed, the timebase tab is labelled 'Rubidium' as seen in Fig. 2.5. The 'Ref Offs' parameter serves the same purpose as the 'OCXO Offs', i.e., adjusting the reference offset. The other parameters are provided for monitoring purposes only.

For instruments with neither of the optional timebases installed, the dedicated timebase tab will be absent. Nevertheless, the internal reference timebase can be adjusted using the 'Ref Offs' parameter that will

in that case be visible on the 'System' tab.

2.7.4 Interface

The CG792 can communicate with remote hosts via RS232, USB, and Ethernet interfaces. The Interface display enables the monitoring and configuration of remote interfaces. The top level Interface display provides information on current configuration of the communication interfaces. A sample display is shown in Figure 2.6.

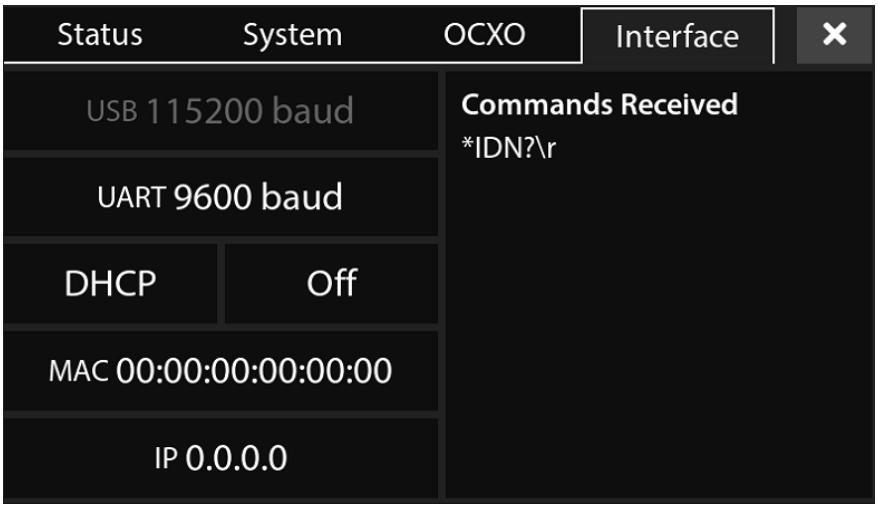


Figure 2.6: Communication Settings

2.7.4.1 RS-232

The CG792 supports communication over an RS-232 port. The rear panel contains a standard 9-pin, female, subminiature-D connector. It is configured as a DCE and supports baud rates from 9,600 to 115,200 baud. The remaining communication parameters are fixed at 8 data bits, 1 stop bit, no parity, with no hardware flow control. The factory default baud rate is 9,600 baud. The baud rate can be adjusted by touching on the 'UART' button in the 'Interface' tab in the Settings window.

2.7.4.2 USB

The CG792 supports communication over the USB protocol as serial device emulation. The rear panel contains a standard Type B connector. The emulated serial port supports the baud rate of 115,200 baud, 8 data bits, 1 stop bit, no parity, with no hardware flow control. The USB parameters are not adjustable.

2.7.4.3 Ethernet

The CG792 may be connected to an Ethernet based local area network (LAN). The rear panel contains a standard RJ-45 connector which accepts Category-5 or Category-6 cable. It supports both 10 and 100 Base-T Ethernet connection speeds.

The following configuration parameters are available from the front panel GUI (see Fig. 2.6):

- **DHCP** Whether to obtain the IP address via DHCP or through a static configuration. Touching this button resets the network interface.
- **IP** The IP address is the one automatically assigned to the device if DHCP is active. If DHCP is disabled, this field allows the user to enter the static IP address. The new value of the static IP address is used after the network interface is reset by touching the DHCP button (above), or by sending the `SYSTem:COMMunicate:LAN:RESet` remote command (see page 78).
- **MAC Address** Every device connected to an Ethernet network must have a unique media access address, or MAC address. This address cannot be changed by the user, but it is sometimes useful to know because some networks use the MAC addresses to identify and regulate which devices can connect to the network. The 'MAC' parameter displays the MAC address in the form '00:19:B3:xx:xx:xx', where the values shown as 'x' are unique to each instrument.

To the right of the screen, a large box displays all the remote commands that the instrument has received from any of the three remote interfaces. Touch the text box to clear it.

TCP/IP Configuration In order to function properly on a TCP/IP network, the CG792 must be configured with a proper IP address. The CG792 supports two different methods of obtaining its network configuration: DHCP and Static IP. The user should check with his network administrator to ascertain the preferred method before connecting the CG792 to a network.

The Ethernet section of the 'Interface' setting tab (Fig. 2.6) shows the method used to obtain the CG792ś current network configuration and its IP address:

- **DHCP** (Dynamic Host Configuration Protocol) is an automated method of obtaining network configuration parameters. In this method the CG792 asks for its configuration from a DHCP server

which then responds with its proper network configuration. Many routers support this configuration method. This is the factory default method of configuration.

- **Static IP** refers to manual configuration. In this method, the user must manually enter the proper network configuration parameters for the CG792 to use.

To select between the two configuration method, either turn DHCP on or off by touching the DHCP parameter value (shown as either 'On' or 'Off'). For example, in Fig. 2.6, the DHCP is currently disabled, so the instrument uses a Static IP configuration.

3 Remote Programming

This chapter describes the operation of the CG792 Multichannel Clock Synthesizer via the remote interfaces.

3.1 Interfaces

The CG792 Multichannel Clock Synthesizer may be programmed via remote interfaces included with the instrument. Any host computer interfaced to the instrument can easily control and monitor its operation. The CG792 supports three standard remote interfaces: RS-232, USB, and an Ethernet based local area network (LAN) interface which supports TCP/IP communication.

The CG792 stores incoming bytes from the remote interfaces in separate input queues. Characters accumulate in the input queue until a command terminator (⟨CR⟩ or ⟨LF⟩) is received, at which point the message is parsed and queued for execution. Queries are returned to the interface from which they were received. If an input queue is full, an error is reported and the data in the queue is discarded.

3.1.1 RS-232

An RS-232 communications port is included on the rear panel of the unit. The RS-232 interface connector is a standard 9 pin, type D, female connector configured as a DCE (transmit on pin 2, receive on pin 3). In order to communicate properly over RS-232, the instrument and the host computer both must be configured to use the same settings. The following baud rates are supported: 115200, 57600, 38400, 19200, and 9600 (default). The rest of the communication parameters are fixed at 8 data bits, 1 stop bit, no parity, and no hardware flow control.

3.1.2 USB

The USB interface via the rear-panel connector is implemented as a serial port emulator. The FTDI drivers for the USB remote interface are well-supported by common operating systems. The drivers will automatically create a virtual RS-232 COM port for communicating with the CG792.

In order to communicate properly over USB, the instrument and the host computer both must be configured to use the same settings. The parameters are fixed as 115,200 baud, 8 data bits, 1 stop bit, no parity, and no flow control.

Characters received cause the front-panel LED labeled 'USB' to flash briefly to indicate interface activity. Note that the LED may flash even if the wrong baud rate is configured on the computer side of the connection. If properly terminated remote commands are sent, and the USB LED flashes, but the instrument does not appear to receive any of the commands, double-check that a baud rate of 115,200 is selected on the computer that is trying to communicate with the CG792.

3.1.3 Ethernet

A rear panel RJ-45 connector may be used to connect the instrument to a 10/100 Base-T Ethernet LAN using the TCP protocol. In order to function properly on an Ethernet LAN, the unit needs to obtain a valid IP address. The CG792 supports two methods for obtaining these parameters: DHCP for automatic IP configuration and Static IP for manual configuration. Check with your network administrator for the proper method of configuration of instruments on your network before attaching the CG792 to your network.

CAUTION

Network security is an important consideration for all TCP/IP networks. Please bear in mind that the CG792 does NOT provide security controls, such as passwords or encryption, for controlling access. If such controls are needed, you must provide it at a higher level on your network. This might be achieved, for example, by setting up a firewall and operating the instrument behind it.

Once connected to the network, the user can connect to the CG792 using a bare TCP stream connection to the instrument's port 5025. All bytes are passed directly to the input queue of the CG792 and all responses sent directly back to the user application. This connection is similar in style to RS-232 connections. Only one Ethernet connection at a time is supported.

Example Python code, assuming the instrument has been assigned the IP address 172.25.70.138:

```
import socket as skt
with skt.socket(skt.AF_INET, skt.SOCK_STREAM) as s:
    s.connect(("172.25.70.138", 5025))
    s.sendall(b"*IDN?\n")
    print(s.recv(1024))
```

If the connection works, each ethernet packet should very briefly light up the front-panel LED labeled 'LAN'. If that does not happen, double check to IP address matches the one reported by the CG792 front-panel, and that the correct port (5025) is used.

3.1.4 Front-Panel Indicators

To assist in programming, there are three front panel indicators located under the 'Interfaces' section of the front panel: USB, LAN, Error. The first two light up momentarily whenever a character is received or transmitted over the corresponding interface. This is useful when troubleshooting connections because it clearly indicates when the CG792 successfully received and responded to a command.

Bit	Name	Meaning
2	ERR	Indicates that one or more errors are present in the error queue. The error may be retrieved with SYST:ERR?.
5	ESB	Standard Event Status Register summary. Set if any bit enabled by the Standard Event Status Enable Register (ESE) is set in the ESR.
6	MSS	Master summary status. This bit is set when any condition enabled in SRE requires service.

Table 3.1: Interpretation of serial poll status bits (STB)

The Error LED will be highlighted when a remote command fails to execute due to illegal syntax or invalid parameters. Once highlighted, the LED will remain lit until the error queue is cleared. Errors may be viewed and cleared either through the GUI (see Section 2.7.1) or using the appropriate remote commands.

3.2 Status Reporting

SCPI defines a standardized status reporting structure consisting of several registers. This instrument implements the *Serial Poll Status Byte (STB)* and the *Standard Event Status Register (ESR)*.

The Serial Poll Status Byte provides summary status information for the instrument. The STB may be queried directly using the *STB? command. The interpretation of the STB bits is given in Table 3.1.

The Standard Event Status Register (ESR) records defined events in the command parser and execution system. Its contents may be queried with the *ESR? command. Reading the ESR clears the register. The implemented bits are listed in Table 3.2.

The ESR interacts with the Serial Poll Status Byte via the Standard Event Status Enable (ESE) register. The ESE register allows software masking of ESR bits to control which events contribute to the ESR summary bit in the STB. The ESE may be set or queried with *ESE and *ESE?, respectively.

3.3 Error Codes

The instrument contains an error buffer that may store up to 10 error codes associated with errors encountered during power-on self tests, command parsing, or command execution. If more than one successive error is the same, only the first one will be reported. The red 'Error' LED will be highlighted when a remote command fails for any reason.

Bit	Name	Meaning
0	OPC	Operation complete. Set when all previously received commands have been executed. This bit is set if the `*OPC` command was issued.
2	QYE	Query error. A query was issued but the response data was not properly read by the controller.
3	DDE	Device dependent error. An instrument-specific error has occurred that is not otherwise classified.
4	EXE	Execution error. A command failed to execute because of an invalid parameter or state.
5	CME	Command error. The parser detected a syntax error in a received command.
7	PON	Power on. Set once after the instrument powers up.

Table 3.2: Interpretation of standard event status bits (ESR)

The errors in the buffer may be read one by one by executing successive `SYST:ERR` commands. The ERR LED will go off when all errors have been discarded. The meaning of each of the error codes is described below.

3.3.1 General Errors

0 No error
The command completed successfully with no errors.

−200 Execution error
A general execution error occurred.

−203 Command protected
The requested command is locked or protected.

−222 Data out of range
The supplied data is outside the valid range.

−225 Out of memory
Not enough memory available to complete the operation.

−241 Hardware missing
A required hardware module was not detected.

−311 Memory error
Nonvolatile memory access failed.

−350 Queue overflow
The error/event queue is full.

3.3.2 Command and Syntax Errors

−113 Invalid command
The command is not recognized.

−115 Param cnt error
Incorrect number of parameters supplied.

−130 Suffix error
A numeric suffix was expected or malformed.

−131 Invalid suffix
The numeric suffix is invalid or unsupported.

3 Command too long
The received command exceeds the maximum length.

18 No entry
The requested command or data entry does not exist.

21 Parameter overflow
A numeric argument exceeded internal limits.

22 Invalid param type
A parameter had the wrong type or format.

23 Invalid units
The specified units are invalid for this parameter.

37 Unknown SCPI error
An unspecified SCPI parser error occurred.

3.3.3 Hardware and Power Supply Errors

1 MPU ADC error
Microcontroller ADC reported an error.

4 Front panel error
General front-panel communication or control error.

5 FP not ready
Front panel not initialized or ready.

6 Front panel 3.3V
Front-panel 3.3 V supply out of range.

7 Front panel 5V
Front-panel 5 V supply out of range.

8 Front panel backl
Front-panel backlight supply out of range.

11 Main PLL error
Error in main LMK/PLL subsystem.

12 Main PLL unlocked
Main PLL failed to lock.

13 5V supply
5 V supply voltage out of range.

14 10V supply
10 V supply voltage out of range.

15 24V supply
24 V supply voltage out of range.

16 1.2V supply
1.2 V supply voltage out of range.

17 N10V supply
−10 V supply voltage out of range.

20 OCXO voltage error
The OCXO supply voltage is outside tolerance.

27 2.5V supply
2.5 V supply voltage out of range.

28 3.3V supply
3.3 V supply voltage out of range.

29 N5V supply
−5 V supply voltage out of range.

30 MPX_GND supply 1
Ground reference 1 abnormal.

31 MPX_GND supply 2
Ground reference 2 abnormal.

32 MPX_VCC supply 1
Power rail MPX_VCC_1 out of range.

33 MPX_VCC supply 2
Power rail MPX_VCC_2 out of range.

36 Rb reference fault
Rubidium frequency reference fault detected.

3.3.4 Network (TCP/IP) Errors

42 TCP: Unknown error
Unspecified TCP error.

43 TCP: Connecting
Connection already being established.

44 TCP: Illegal arg

Invalid argument to TCP API.

45 TCP: Buffer error
Transmit or receive buffer error.

46 TCP: Low level err
Low-level network interface error.

47 TCP: In progress
A connection is already in progress.

48 TCP: Conn already
Socket already connected.

49 TCP: Out of memory
TCP/IP stack ran out of memory.

50 TCP: Routing error
No valid route to destination.

51 TCP: Address in use
Requested address or port already in use.

52 TCP: Illegal value
Invalid argument to a TCP call.

53 TCP: Blocking op
Operation would block (non-blocking socket).

3.3.5 Timing, Control, and Synchronization Errors

2 UART baud rate
Invalid or unsupported UART baud rate.

9 Frequency too high
Requested frequency above valid range.

10 Frequency too low
Requested frequency below valid range.

17 Mutex timeout
A mutex or semaphore timed out.

19 PLL param calc
Numerology or PLL parameter calculation failed.

41 Sync error
System synchronization failed.

3.3.6 Modulation and Phase-Shift Errors

13 Modulation limit
Requested modulation parameters invalid.

14 Clock disabled: modulation not allowed
Cannot enable modulation while the clock is disabled.

15 Mod period fixed
Modulation period cannot be changed in this mode.

16 PRBS active: modulation not allowed
Cannot enable modulation while PRBS is active.

38 Clock disabled: phase shift not allowed
Phase shift requested on a disabled clock.

39 Modulation active: phase shift not allowed
Phase shift cannot be applied while modulation is active.

40 PRBS active: phase shift not allowed
Phase shift cannot be applied during PRBS operation.

3.4 SCPI Command Language

The CG792 uses the SCPI (Standard Commands for Programmable Instruments) language for controlling the instrument over a remote interface. The SCPI language is an ASCII-based command language that organizes functions into a hierarchical tree of commands with branches of the tree separated by colons.

3.4.1 Subsystems

The base or root of the tree represents a subsystem of the instrument. Each succeeding branch of the tree subdivides the subsystem into related categories of functionality. The final branch of the tree identifies a command related to the subsystem that can be executed by the CG792. This structure facilitates understanding of the functions carried out by commands.

3.4.2 Understanding Command Syntax

SCPI commands often take one or more parameters which modify or identify the numerical value a variable should take. Some parameters are required. Others may be optional. Furthermore, the data types for each parameter may differ. Thus, for brevity, we need a set of conventions for defining commands which clearly identifies all the valid variations of the command without having the list each possibility separately. These conventions are set forth here.

Two example commands are illustrated below:

```
[SOURce[1|2|3|4]]:STATe {ON|OFF}
```

```
[SOURce[1|2|3|4]]:STATe?
```

3.4.2.1 Keyword Case

Keywords are defined with a mixture of upper-case and lower-case letters. The upper-case letters indicate the short or abbreviated version of the keyword. This is usually the first three or four letters of the keyword. The user may send either the short version or the entire long version of the keyword in their programs. The case of the letters sent to the CG792 does not matter. It is only used here to succinctly identify the two versions of the keyword. Thus, `SOUR`, `source`, and `Sour` are all acceptable forms of the keyword. Other forms, such as `SOU`, or `SOURC`, are not.

3.4.2.2 Punctuation Used in Definitions

The following punctuation is used to identify variations and options for the command:

- Braces (`{ }`) enclose different parameter choices. The braces, themselves, are not sent with the command.
- A vertical bar (`|`) separates alternative parameter choices for the command. The vertical bar is not sent with the command.
- Triangle brackets (`< >`) indicate that you must specify a numerical value. For example, `<voltage>` would be specified as a number. The triangle brackets are not sent with the command.
- Square brackets (`[ ]`) identify optional keywords or parameters in the command. Optional items may be omitted if desired. In such case a default value is normally substituted for the parameter.

3.4.2.3 Numeric Suffix

Some keywords can have a numeric suffix appended to the keyword. For example, `SOURce` may be followed with a `1` or `2`. These suffixes identify multiple channels of the same subsystem. Thus, `SOUR1` identifies channel 1, and `SOUR2` identifies channel 2. The numeric suffix is optional and if omitted, channel 1 is assumed. No space is permitted between the command and the numeric suffix.

3.4.2.4 Queries

Command queries are usually formed by appending a question mark (`?`) to the appropriate set command. For example, query the state of channel 1, we use the following command: `SOURce1:STATe?`.

3.4.2.5 Separators

As mentioned above, a colon (:) separates the different keywords that make up a command. If a command takes a parameter, a space must separate the last keyword of a command and the first parameter of that command. If a command takes multiple parameters, they are separated from each other with a comma (,). Finally, a semicolon (;) is used to separate multiple commands on the same line. If the following command is in the same subsystem as the preceding command then the subsystem is not repeated for the second command. Otherwise the command must be fully specified and preceded by a colon.

3.4.2.6 Sending Multiple Commands

There are three ways of sending multiple commands:

1. Send the commands as separate messages, each line ends with a a terminator character (⟨CR⟩ or ⟨LF⟩):

   ```
   SOURCE2:FREQ 10e6;

   SOURCE2:PHAS 180;
   ```

2. Send them as one long line. Make sure to separate the commands with both a semicolon and a colon (the first command does not need the colon):

   ```
   SOURCE2:FREQ 10e6;:SOURCE2:PHAS 180;
   ```

3. One short message, where the commands are not separated with colons, only semicolons. The messages have to be on the same level, since without the colon the parser does not reset to the root of the command tree. For example, the following is identical to the previous example:

   ```
   SOURCE2:FREQ 10e6;PHAS 180;
   ```

   Note that `PHAS 180` applies to `SOURCE2` and not `SOURCE1`, since the starting semicolon has been omitted.

3.4.2.7 IEEE 488.2 Common Commands

The IEEE 488.2 standard defines several common commands that nearly all instruments support. Common commands start with an asterisk (*) followed by three letters. Like with SCPI commands, a space must separate the command and any parameters which follow. Multiple common commands may executed in a single line by separating the commands with a semicolon (;). An example is given below.

```
*RST; *OPC?
```

3.4.3 Parameter Types

The SCPI language supports several different data types for use with command parameters.

3.4.3.1 Numeric Values

Parameters that take numeric values accept all common decimal representations of numbers, including optional signs, decimal points, or scientific notation. If only certain values are allowed, numeric entries will be rounded to the nearest allowed value. The following examples are all valid numeric entries:

```
100

-123.456

+1.23456e2

-.456
```

3.4.3.2 Supported Units

Since the command set is case-insensitive, the SI unit prefixes are ambiguous (mHz and MHz would be the same unit). To avoid ambiguity, this instrument supports only the base units: hertz (Hz), volts (V), seconds (s), degrees Celsius (C), and degrees (deg). However, the values are to be entered using base-10 exponents; for example, `300e6 Hz` would be 300 MHz. The unit itself is not needed; the frequency can thus be set with the `FREQ 300e6` command.

3.4.3.3 Discrete Parameters

Some parameters take one of a small list of allowed keywords. They often have a short form and a long form, just like command keywords. In the command definition, the upper case letters indicate the short form. Either case may be used when sending the short or long form of the value to the instrument. Queries will always return the short form.

3.4.3.4 Command Termination

Commands should be terminated with a line feed ⟨LF⟩ or carriage return ⟨LF⟩. They may optionally be terminated with a carriage return ⟨CR⟩ followed by a line feed ⟨LF⟩. As previously noted, multiple commands may be sent in a single line if they separated by a semicolon (;). Commands are executed in the order received and execution commences once the terminator is received.

3.5 Command Description

Remote operation of the CG792 is through a simple SCPI-like command language documented in this section. Both set and query forms of most commands are supported, allowing the user complete control of the unit from a remote computer through RS-232, USB, or Ethernet interfaces.

The next section contains a detailed description of the command syntax, arguments, return values, and usage examples. Refer to the index of commends on page 8 for an overview.

Unless otherwise noted, the return values are only applicable for the query form of each command, while the arguments are only applicable for the set command. Thus the set commands do not return any values and the query commands do not take any arguments. For a command with multiple arguments or return values, these are separated by commas (,).

If a set command takes a number of different text-based options (for example, `ON` and `OFF`), the query command will return the result using the same text. Thus only the set arguments are described, since the query return values have the same meaning.

3.5.1 Common Commands

Provides standard SCPI commands for instrument control, including clearing status, querying errors, identifying the instrument, resetting, and managing stored states. These commands are essential for basic communication and status monitoring.

***CLS** **Clear Status**

Clear the event register in all register groups and the error queue (`SYST:ERR`).

Syntax: `*CLS`

3.5.1 Common Commands (continued)

***ESE[?]** **Event Status Enable**

Set the Standard Event Status Enable register. Bits set in this register cause ESB (in *STB) to be set when the corresponding bit is set in the *ESR register. The query returns the current value of the enable register.

Syntax: `*ESE <value>`

`*ESE?`

Arguments: `<value>` Event Status Enable register value. The value may range from 0 to 255.

For example, to enable bits 1, 2, and 7, set value to $2^1 + 2^2 + 2^7 = 134$.

Return values: `<value>` Event Status Enable register value (see above).

***ESR?** **Event Status Register**

Query the Standard Event Status register. The response is the decimal sum of the latched bits in the standard event status register.

Bits in the Standard Event Status register remain set until they are cleared by reading with the `*ESR?` command, or by sending `*CLS` to clear the register.

The bits in the ESR register have the following meaning:

Bit	Name	Meaning
0	OPC	Operation complete
1	—	*(Reserved)*
2	QYE	Query error
3	DDE	Device dependent error
4	EXE	Execution error
5	CME	Command error
6	—	*(Reserved)*
7	PON	Power-on

Syntax: `*ESR?`

Return values: `<value>` Event Status register value.

3.5.1 Common Commands (continued)

***IDN?** **Identify**

Query the CG792 identification string.

Syntax: `*IDN?`

Return values: *Stanford Research Systems*

<*model*> Model number, *CG792*.

<*sn*> Instrument serial number.

<*ver*> Firmware version.

<*opts*> Installed options.

Example: `*IDN?`
Stanford Research Systems,CG792,s/n00000005,ver1.000,Rb,n3,n4

***OPC[?]** **Operation Complete**

The set form sets the OPC flag in the ESR register when all prior commands have completed.

The query form returns *1* when all prior commands have completed, but does not affect the ESR register.

Syntax: `*OPC`

`*OPC?`

Return values: The response will be *1* if the commands have finished executing, or *0* if not.

***RCL** **Recall Instrument Settings**

Recall instrument settings from <location>. The <location> may range from 0 to 8. Locations 1 to 7 are for arbitrary use. Location 0 is reserved for the recall of startup instrument settings. Location 8 recalls factory default settings.

Syntax: `*RCL <location>`

***RST** **Reset**

Restore factory-default settings. Equivalent to `*RCL 8`.

Syntax: `*RST`

3.5.1 Common Commands (continued)

***SAV** **Save Instrument Settings**

Save instrument settings to <location>. The <location> may range from 0 to 7. However, location 0 is reserved for current instrument settings.

Syntax: *SAV <location>

***SRE[?]** **Service Request Enable**

Set or query the Service Request Enable register.

Each bit in the SRE corresponds one-to-one with a bit in the SB register, and acts as a bitwise AND of the SB flags to generate MSS. Bit 6 of the SRE is undefined—setting it has no effect, and reading it always returns 0.

At power-on, this register is cleared.

Syntax: *SRE <value>

*SRE?

Arguments: <value> Register value. The value may range from 0 to 255.

Return values: <value> Register value. The value may range from 0 to 255.

***STB** **Status Byte**

Query the standard IEEE 488.2 serial poll status byte.

The bits in the STB register have the following meaning:

Bit	Name	Meaning
0		*(Reserved)*
1		*(Reserved)*
2	ERR	Error queue is not empty
3		*(Reserved)*
4		*(Reserved)*
5	ESB	Summary of ESR register
6	MSS	Master summary bit
7		*(Reserved)*

Bits must be enabled in the status request enable register (see *SRE) to be reported in the status byte register. Bits in the status byte are updated in real time and bits are not cleared when read. Power cycling or a device reboot (SYSTem:REBoot) will clear the status byte.

Syntax: *STB?

Return values: <value> Register value. The value may range from 0 to 255.

3.5.1 Common Commands (continued)

***TST?** **Test**

Perform a self-test of the instrument and return a summary of the results. This is the same self-test that is performed at instrument startup.

Syntax: `*TST?`

Return values: *{PASS|FAIL}* Report if the instrument passed or failed the tests.

***WAI** **Wait**

The instrument will not process further commands until all prior commands including this one have completed.

Note that since the CG792 executes all commands sequentially, this command has no effect.

Syntax: `*WAI`

3.5.2 Error & Info

Commands in this section allow querying and clearing the error queue, as well as obtaining system information such as memory usage, internal temperature, uptime, and supply voltages. This helps with diagnostics and system monitoring.

SYSTem:REBoot **Reboot**

Reboot the CG792. Does not save instrument settings.

Syntax: `SYSTem:REBoot`

SYSTem:ERRor:CLEAR **Clear error queue**

Clears all entries from the system error queue.

Syntax: `SYSTem:ERRor:CLEAR`

Example: Use this command to reset the error queue before running a test sequence:

```
SYST:ERR:CLEAR
```

3.5.2 Error & Info (continued)

SYSTem:ERRor[:NEXT]? **Query next error in queue**

Queries and removes the next message from the system error queue. Returns the error code and its text message.

Syntax: `SYSTem:ERRor?`

Return values: `<code>,<message>` Numeric error code and its descriptive text.

Example: Query and clear the first pending error:

```
SYSTem:ERR:NEXT?
```

SYSTem:FACToryreset **Factory Reset**

Resets the instrument to the factory default configuration. All stored information and memory locations, including communication parameters, are cleared and set to the factory defaults.

Syntax: `SYSTem:FACT`

SYSTem:INFO:MEMory? **Query memory usage**

Queries the instrument's current memory utilization.

Syntax: `SYSTem:INFO:MEMory?`

Return values: `<mpu>,<fp>` MPU and front-panel free memory in bytes.

Example: Check remaining memory capacity:

```
SYST:INFO:MEM?
```

SYSTem:INFO:TEMPerature? **Query internal temperature**

Queries the instrument's internal temperature sensors.

Syntax: `SYSTem:INFO:TEMPerature?`

Return values: `<mpu>,<fp>` MPU and front-panel processor temperature in degrees Celsius.

Example: Measure internal temperature for diagnostic purposes:

```
SYST:INFO:TEMP?
```

3.5.2 Error & Info (continued)

SYSTem:INFO:UPTime? **Query system uptime**

Returns the time elapsed since the last system reset or power-on.

Syntax: `SYSTem:INFO:UPTime?`

Return values: <time> Uptime in seconds.

Example: Query how long the instrument has been running:

```
SYST:INFO:UPT?
```

3.5.2 Error & Info (continued)

SYSTem:INFO:VOLTage? **Query supply voltages**

Queries the current supply voltage readings of internal power rails.

Syntax: `SYSTem:INFO:VOLTage?`

Return values: `<v0>,<v1>,<v2>,<v3>,<v4>,<v5>,<v6>,<v7>,<v8>,<v9>,<v10>,<v11>,<v12>,<v13>,<v14>`

v0 Power rail MPX VCC front voltage.

v1 Power rail MPX GND front voltage.

v2 Power rail MPX VCC rear voltage.

v3 Power rail MPX GND rear voltage.

v4 Motherboard 24 V supply voltage.

v5 Motherboard 10 V supply voltage.

v6 Motherboard 5 V supply voltage.

v7 Motherboard 3.3 V supply voltage.

v8 Motherboard 2.5 V supply voltage.

v9 Motherboard 1.2 V supply voltage.

v10 Motherboard −5 V supply voltage.

v11 Motherboard −10 V supply voltage.

v12 Front panel 3.3 V supply voltage.

v13 Front panel 5 V supply voltage.

v14 Front panel backlight supply voltage.

Example: Verify the health of the internal power supplies:

```
SYST:INFO:VOLT?
```

```
4.279,0.996,0.000,0.000,23.987,9.975,5.013,3.178,2.500,1.200,-4.986,-9.980,3.223,5.073,0.017
```

3.5.2 Error & Info (continued)

SYSTem:BEEP **Set/query beep loudness**

Sets or queries the loudness of the beep sound upon system boot or GUI touch or button press. The query form returns the current frequency in hertz.

Syntax: `SYSTem:BEEP <Bol>`

`SYSTem:BEEP?`

Arguments: `<bol>` Loudness, either `OFF`, **`LOW`** (default), or `HIGH`.

3.5.3 Source

Controls the signal output, including frequency, phase, amplitude, offset, and enabling or disabling the output. Also allows querying the installed source module and aligning output phases.

SOURce#:FREQuency[?] **Set/query output frequency**

Sets or queries the output frequency of source channel `#`. The query form returns the current frequency in hertz. The default value is **10e6**.

Syntax: `SOURce#:FREQuency <value>`

`SOURce#:FREQuency?`

Arguments: `<value>` Output frequency in hertz. Range: `1e-3` to `2.2e9`.

Return values: `<value>` Current frequency setting in hertz.

Example: Set the first source to 10 MHz and verify:

```
SOUR1:FREQ 10e6
SOUR1:FREQ?
```

3.5.3 Source (continued)

SOURce#:FASTfrequency — **Set frequency, quickly**

Sets the output frequency of source channel #, approximately two times faster than the regular `SOURce#:FREQuency` command.

This command comes with the limitation that modulation and mode changes must not be used after `FASTfrequency` command; the behavior in that case is undefined since the command disables regular parameter checking. It is intended only for frequency changes. It is recommended to do a full reset and reboot after using this command to restore full instrument functionality.

Syntax: `SOURce#:FAST <value>`

Arguments: `<value>` Output frequency in hertz. Range: `1e-3` to `2.2e9`.

SOURce#:INST? — **Query installed source module**

Queries whether the source module is installed in position #.

Syntax: `SOURce#:INST?`

Return values: *0* If channel is not installed.

1 If channel is installed.

Example: Check the installed source type:

```
SOUR1:INST?
```

SOURce#:PHASe[?] — **Set/query output phase**

Sets or queries the phase offset of the specified source channel in degrees. The query version of the command returns the value with the number of decimal places limited in accordance with the resolution specified on page 3. Default value: **0**.

Syntax: `SOURce#:PHASe <value>`

`SOURce#:PHASe?`

Arguments: `<value>` Phase offset in degrees. Range: `-720` to `720`.

Return values: `<value>` Current phase setting in degrees.

Example: Shift the output phase to 90°:

```
SOUR1:PHAS 90
```

3.5.3 Source (continued)

SOURce#:EXTPhase? **Query precise phase**

Queries the phase offset of the specified source channel in degrees. Unlike `SOURce#:PHASe?`, it always returns the output with 15 decimal places. Default value: **0.000000000000000**.

Syntax: `SOURce#:EXTPhase?`

Return values: `<value>` Current phase setting in degrees.

SOURce#:REL **Define phase as zero**

Sets the current value of the phase as the new zero point for the phase. Regardless of what phase value is displayed, after receving this command, the value will be zero. This command does not change the clock outputs, just redefines the zero point.

Syntax: `SOURce#:REL`

3.5.3 Source (continued)

SOURce#:STATe[?] — **Enable/disable/query output state**

Enables, disables, or modifies the output mode of source channel #. The query form returns the current state.

Syntax: `SOURce#:STATe <state>`

`SOURce#:STATe?`

Arguments: `<state>` One of `OFF`, **`ON`** (default), `INV`, `BLANK`, `PRBS`, `LOW`, `HIGH`.

`OFF`. Disable selected clock channel, and set its output to zero volts.

`ON`. Enable selected clock channel.

`INV`. Enable selected clock channel, and set the differential outputs to be inverted when the external digital modulation input is asserted.

`BLANK`. Enable selected clock channel, and set the CMOS and differential outputs to be blanked when the external digital modulation input is asserted.

`PRBS`. Enable selected clock channel, and configure it to output a pseudo-random bit sequence.

`LOW`. Disable selected clock channel, and set its output to the LOW polarity.

`HIGH`. Disable selected clock channel, and set its output to the HIGH polarity.

Return values: `<state>` Current output state.

Example: Enable source 1:

```
SOUR1:STAT ON
```

SOURce#:SYNC — **Align phase of outputs**

Synchronizes the phase of a selected source outputs to a common reference. Please review the limitations described in Section 2.5 (page 37) on which channels may be synchronized to each other.

Syntax: `SOURce#:SYNC <ch>`

Arguments: `<ch>` Which output channel to sync to.

Example: Synchronize channels 1 to channel 2, such that the frequency and phase of channel 1 is adjusted until it matches that of channel 2:

```
SOUR1:SYNC 2
```

3.5.3 Source (continued)

SOURce#:VOLTage:AMPLitude[?] **Set/query output amplitude**

Sets or queries the differential output amplitude (peak-to-peak) in volts. Default value: **1.0**.

Syntax: `SOURce#:VOLTage:AMPLitude <value>`

`SOURce#:VOLTage:AMPLitude?`

Arguments: `<value>` Output amplitude in volts. Range: `0` to `1.2`.

Return values: `<value>` Current amplitude in volts.

Example: Set source 1 amplitude to 0.8 V_{pp}:

```
SOUR1:VOLT:AMPL 0.8
```

SOURce#:VOLTage:OFFSet[?] **Set/query DC offset**

Sets or queries the DC offset voltage of the differential output signal. Default value: **0.0**.

Syntax: `SOURce#:VOLTage:OFFSet <value>`

`SOURce#:VOLTage:OFFSet?`

Arguments: `<value>` DC offset in volts. Range: `-3` to `2`.

Return values: `<value>` Current offset in volts.

Example: Apply a +1.2 V offset to source 1 output:

```
SOUR1:VOLT:OFFS 1.2
```

3.5.4 Modulation

Configures modulation parameters such as mode, type, period, polarity, sample rate, and blanking. This section defines how the output signal is modulated.

3.5.4 Modulation (continued)

MODulation:MODE[?] — **Set/query modulation mode**

Selects or queries the current modulation mode. The modulation mode determines whether the signal output is unmodulated or uses FM, PM, or jitter modulation.

Syntax: `MODulation:MODE <mode>`

`MODulation:MODE?`

Arguments:

OFF	Modulation disabled (default).
FM	Frequency modulation.
PM	Phase modulation.
JITTER	Jitter modulation.

Example: Enable phase modulation:

```
MODulation:MODE PM
```

MODulation:PERiod[?] — **Set/query modulation period**

Sets or queries the modulation period. The period defines the duration of one complete modulation cycle. Default value: **1.0**.

Syntax: `MODulation:PERiod <seconds>`

`MODulation:PERiod?`

Arguments:

<seconds>	Real, 0.1 ms to 5 s.

Example: Set modulation period to 2 ms:

```
MODulation:PERiod 2E-3
```

MODulation:PERiod:ACTual? — **Query effective modulation period**

Queries the effective modulation period currently in use, including any quantization or hardware rounding.

Syntax: `MODulation:PERiod:ACTual?`

Return values: *<seconds>* Effective modulation period.

3.5.4 Modulation (continued)

MODulation:BLANk[?] — **Enable/disable/query blanking**

Enables, disables, or queries modulation blanking. When blanking is enabled, the modulation can be momentarily zeroed by asserting the external digital modulation input.

Syntax:
```
MODulation:BLANk ON|OFF

MODulation:BLANk?
```

Arguments:

`ON`	Blanking enabled.
`OFF`	Blanking disabled (default).

Example: Enable modulation blanking:

```
MODulation:BLANk ON
```

MODulation:POLarity[?] — **Set/query modulation polarity**

Sets or queries the blanking polarity. This determines whether the clock signal is held in the HIGH or LOW state when blanking is asserted, when blanking is enabled.

Syntax:
```
MODulation:POLarity <state>

MODulation:POLarity?
```

Arguments:

`0`	Blank LOW (default).
`1`	Blank HIGH.

Example: Set to blank HIGH, when blanking enabled and asserted:

```
MODulation:POLarity 1
```

MODulation:RATE[?] — **Set/query modulation sample rate**

Sets or queries the modulation sample rate. This defines the rate at which modulating waveform samples are generated or applied.

Syntax:
```
MODulation:RATE <rate>

MODulation:RATE?
```

Arguments: `<rate>` Sample rate in samples per second. The range depends on other modulation settings.

Example: Set modulation sample rate to 50 kHz:

```
MODulation:RATE 50E3
```

3.5.4 Modulation (continued)

MODulation:TYPE[?] **Set/query modulation type**

Selects or queries the modulation waveform type.

Syntax: `MODulation:TYPE <type>`

`MODulation:TYPE?`

Arguments:

`SINe`	Sine wave modulation (default).
`TRIangle`	Triangle waveform.
`RAMP`	Ramp or sawtooth.
`SQUare`	Square waveform.
`NOISe`	Pseudo-random noise.
`EXTernal`	External analog modulation.

Example: Select triangle modulation:

```
MODulation:TYPE TRIangle
```

SOURce#:MODulation:DEViation[?] **Set/query modulation deviation**

Sets or queries the modulation deviation for the specified source channel. Deviation specifies the maximum frequency or phase shift from nominal. Default value: **0.0**.

Syntax: `SOURce#:MODulation:DEViation <dev>`

`SOURce#:MODulation:DEViation?`

Arguments: `<dev>` Modulation deviation. For FM, the value is understood as ppm of the carrier (range: 0 to 75 ppm). For phase modulation, the modulation deviation is in seconds per volt of external analog input; the range depends on the sample rate.

Example: Set channel 1 modulation deviation to 25 ppm:

```
SOURce1:MODulation:DEViation 25E-6
```

3.5.4 Modulation (continued)

SOURce#:MODulation:JITTer[?] — **Set/query jitter enable state**

Enables, disables, or queries jitter modulation for the specified source channel.

Syntax: `SOURce#:MODulation:JITTer ON|OFF`

`SOURce#:MODulation:JITTer?`

Arguments:

`ON` Enable jitter modulation.
`OFF` Disable jitter modulation (default).

Example: Enable jitter modulation on source 2:

```
SOURce2:MODulation:JITTer ON
```

MODulation:JITTer[?] — **Set/query jitter magnitude**

Sets or queries the peak-to-peak jitter magnitude in seconds. This value determines the temporal modulation extent. Default value: **0**.

Syntax: `MODulation:JITTer <seconds>`

`MODulation:JITTer?`

Arguments: `<seconds>` Real, 0 to 3 ms.

Example: Set jitter magnitude to 1 ms:

```
MODulation:JITTer 1E-3
```

3.5.5 Communication (continued)

MODulation:ZERO — **Pause or resume modulation**

Immediately pauses or resumes modulation output without altering settings. Note that this command does not modify the parameters as displayed on the front panel or which can be queried from the front panel. When using this command, make sure to remember whether the modulation has been paused or resumed, or simply reload the other modulation settings if not sure.

Syntax: `MODulation:ZERO <state>`

Arguments:

0 Resume modulation.
1 Pause modulation.

Example: Pause modulation output:

```
MODulation:ZERO 1
```

3.5.5 Communication

Manages network and serial interfaces, including DHCP, IP and MAC addresses, link status, and baud rates. Ensures proper setup and monitoring of LAN, USB, and serial communication.

SYSTem:COMMunicate:LAN:DHCP[?] — **Enable/disable/query DHCP**

Enables, disables, or queries DHCP operation on the LAN interface. When DHCP is enabled, the instrument obtains its IP configuration automatically from a DHCP server.

Syntax: `SYSTem:COMMunicate:LAN:DHCP ON|OFF`

`SYSTem:COMMunicate:LAN:DHCP?`

Arguments:

ON Enable DHCP client operation (default).
OFF Disable DHCP and use static addressing.

Example: Disable DHCP to enable manual IP configuration:

```
SYSTem:COMMunicate:LAN:DHCP OFF
```

3.5.5 Communication (continued)

SYSTem:COMMunicate:LAN:DHCP:STATus? **Query DHCP lease status**

Queries the current DHCP lease state and assigned address information, if applicable.

Syntax: `SYSTem:COMMunicate:LAN:DHCP:STATus?`

Return values: <*string*> DHCP lease status description.

SYSTem:COMMunicate:LAN:IPADdress[?] **Set/query IP address**

Sets or queries the static IP address used by the LAN interface when DHCP is disabled.

Syntax: `SYSTem:COMMunicate:LAN:IPADdress <value>`

`SYSTem:COMMunicate:LAN:IPADdress?`

Arguments: <value> IP address in the usual "dot" notation (0.0.0.0 to 255.255.255.255).

Example: Set the static IP address to 192.168.0.100:

`SYSTem:COMMunicate:LAN:IPADdress 192.168.0.100`

SYSTem:COMMunicate:LAN:MAC? **Query MAC address**

Queries the factory-assigned MAC address of the LAN interface.

Syntax: `SYSTem:COMMunicate:LAN:MAC?`

Return values: <*string*> MAC address in standard colon-separated format.

SYSTem:COMMunicate:LAN:RESet **Reset LAN interface**

Resets the LAN interface to apply new network settings or recover from communication errors. The network connection will temporarily drop during the reset.

Syntax: `SYSTem:COMMunicate:LAN:RESet`

Example: Restart the LAN interface to apply new static IP settings:

`SYSTem:COMMunicate:LAN:RESet`

SYSTem:COMMunicate:LAN:STATus? **Query LAN link status**

Queries the current link state and connection information of the LAN interface.

Syntax: `SYSTem:COMMunicate:LAN:STATus?`

Return values: <*string*> Link status string, either 'Connected' or 'Disconnected'.

3.5.5 Communication (continued)

SYSTem:COMMunicate:SERial:BAUD[?] — **Set/query serial baud rate**

Sets or queries the baud rate of the serial (RS-232) interface.

Syntax:
```
SYSTem:COMMunicate:SERial:BAUD <value>
SYSTem:COMMunicate:SERial:BAUD?
```

Arguments:

<value> Integer, one of 115200, 57600, 38400, 19200, and **9600** (default).

Example: Set the serial interface to 115200 baud:

```
SYSTem:COMMunicate:SERial:BAUD 115200
```

SYSTem:COMMunicate:USB:BAUD? — **Query USB virtual COM baud rate**

Queries the effective baud rate reported by the USB virtual COM interface. The value is always 115200.

Syntax:
```
SYSTem:COMMunicate:USB:BAUD?
```

Return values: *115200* USB serial baud rate in bits per second.

3.5.6 Display Backlight

Adjusts display settings, including brightness level and automatic turn-off timing. These commands control user interface visibility and power management.

SYSTem:DISPlay:LEVel[?] — **Set/query display brightness**

Sets the display brightness level or queries the current brightness. Values are given as a percentage of maximum brightness. Default value: **50**.

Syntax:
```
SYSTem:DISPlay:LEVel <value>
SYSTem:DISPlay:LEVel?
```

Arguments:

<value> Brightness level from 20 to 100 (%).

Example: Set display brightness to maximum:

```
SYSTem:DISPlay:LEVel 100
```

3.5.6 Display Backlight (continued)

SYSTem:DISPlay:OFF[?] — **Turn display on/off**

Turns the display off, on, or sets an auto-off timer. Queries return the current display state.

Syntax: `SYSTem:DISPlay:OFF <state>`

`SYSTem:DISPlay:OFF?`

Arguments:

`OFF`	Turn display off immediately.
`ON`	Turn display on (default).
`MIN`	Auto-off after 1 minute.
`1H`	Auto-off after 1 hour.
`2H`	Auto-off after 2 hours.
`4H`	Auto-off after 4 hours.
`8H`	Auto-off after 8 hours.
`DAY`	Auto-off after 1 day.
`WEEK`	Auto-off after 1 week.

Example: Turn the display off for 2 hours:

```
SYSTem:DISPlay:OFF 2H
```

3.5.7 Timebase / Reference

Configures and monitors the internal and external frequency references, including OCXO, rubidium, and TCXO sources. Allows trimming frequency, checking lock status, and monitoring temperatures and control signals for precision timing.

SYSTem:REFerence:LOCK? — **Query reference lock status**

Returns whether the current reference oscillator is locked.

Syntax: `SYSTem:REFerence:LOCK?`

Return values: `<state>` 'LOCKED' or 'UNLOCKED'

SYSTem:REFerence:EXTernal:STATus? — **Query external reference voltage**

Reports the status of the external reference input voltage.

Syntax: `SYSTem:REFerence:EXTernal:STATus?`

Return values: `<value>` External reference voltage in volts.

3.5.7 Timebase / Reference (continued)

SYSTem:REFerence:INTernal:TYPe? **Query internal reference type**

Returns the type of internal reference oscillator (e.g., OCXO, Rubidium, TCXO).

Syntax: `SYSTem:REFerence:INTernal:TYPe?`

Return values: *<string>* Internal reference type.

SYSTem:REFerence:OCXO:FCONtrol[?] **Set/query OCXO frequency trim**

Adjusts or queries the frequency trim of the OCXO. Default value: **0.0**.

Syntax: `SYSTem:REFerence:OCXO:FCONtrol <value>`

`SYSTem:REFerence:OCXO:FCONtrol?`

Arguments: <value> Frequency trim from -0.4e-6 to +0.4e-6.

SYSTem:REFerence:OCXO:AGC? **Query OCXO AGC status**

Returns the current automatic gain control status of the OCXO.

Syntax: `SYSTem:REFerence:OCXO:AGC?`

Return values: *<state>* 'ON' or 'OFF'

SYSTem:REFerence:OCXO:HEAT? **Query OCXO heater status**

Returns whether the OCXO heater is active.

Syntax: `SYSTem:REFerence:OCXO:HEAT?`

Return values: *<state>* 'ON' or 'OFF'

SYSTem:REFerence:OCXO:VARac? **Query OCXO varactor status**

Reports the current varactor tuning voltage of the OCXO.

Syntax: `SYSTem:REFerence:OCXO:VARac?`

Return values: *<value>* Varactor voltage in volts.

SYSTem:REFerence:RB:FCONtrol[?] **Set/query rubidium frequency trim**

Adjusts or queries the rubidium reference frequency trim. Default value: **0.0**.

Syntax: `SYSTem:REFerence:RB:FCONtrol <value>`

`SYSTem:REFerence:RB:FCONtrol?`

Arguments: <value> Trim from -2000 to +2000.

3.5.7 Timebase / Reference (continued)

SYSTem:REFerence:RB:STATus? **Query rubidium status code**

Returns the status code of the rubidium reference.

Syntax: `SYSTem:REFerence:RB:STATus?`

Return values: *<code>* Status code integer.

SYSTem:REFerence:RB:TEMP#? **Query rubidium temperature sensor**

Reads the temperature from the rubidium reference sensor.

Syntax: `SYSTem:REFerence:RB:TEMP#?`

Return values: *<value>* Temperature in degrees Celsius.

SYSTem:REFerence:TCXO:FCONtrol[?] **Set/query TCXO frequency trim**

Adjusts or queries the frequency trim of the TCXO. Default value: **0.0**.

Syntax: `SYSTem:REFerence:TCXO:FCONtrol <value>`

`SYSTem:REFerence:TCXO:FCONtrol?`

Arguments: <value> Trim from -49999e-9 to +49999e-9.

Appendix A Frequency Synthesis

This chapter explains the working principles behind the frequency synthesis technique used in the CG792 Multichannel Clock Synthesizer.

A.1 Instrument Overview

The CG792s are multichannel clock synthesizers which operate from DC to 2.2 GHz. The standard instrument has two front panel clock channels and can be ordered with one, or two, additional clock channels on the rear panel. Sketches of the front and rear panels for the CG792 (with optional rear panel clock channels installed) are shown below.

The instrument's standard timebase is a TCXO, with OCXOs and Rb standards available as options. The internal timebase can be locked to a user-applied external 10 MHz timebase. The instrument's motherboard provides one of four reference frequencies, between 62 MHz and 100 MHz (chosen so as to avoid synthesizer spurs), to each of the four clock channels cards.

A.2 Spur Avoidance

There are several important issues to consider in the design of the frequency synthesizer chain for the clock generator. Key among those considerations is the avoidance of integer boundary spurs (IBSs) which occur when fractional-N dividers get close to integer boundaries. We use the LMK05318B integrated circuit to generate reference frequencies for up to four LMX2572 Clock output synthesizers, selecting the VCO frequency and output dividers so as to avoid IBSs.

In this plan, the XO is a 24.576 MHz TCXO, which is a common, low-cost crystal oscillator, that will serve as the standard timebase for the Clock Synthesizer. The XO controls the short-term stability of APLL1, but it may also be disciplined to an optional timebase or external timebase input. To do so we use the DPLL feature of the LMK05318B to lock VCO1 to either the external 10 MHz timebase input (via PRIREF) or an optional timebase (OCXO or Rb, via SECREF) with a bandwidth of a few 100 Hz.

The LMK05318B has two APLLs. Both APLLs have low phase noise.

APLL1 has a narrow band 2,500 MHz BAW VCO with very low phase noise. This VCO will be locked to the XO input using an N-value of about 92.592, nicely away from integer and half-integer boundaries. The output divider will be set to either 25 or 40 to provide output frequencies of 100 MHz or 62.5 MHz.

The reference frequency to APLL2 will be 100 MHz, sourced from APLL1 by dividing with RP=5 and RS=5. We will lock APLL2 to 6,200 MHz, just below its top frequency of 6,250 MHz, by using an integer divider of 62. The post-divider for APLL2 output will be set to 2, and the output divider will be set to 40 or 50 to provide a reference clock outputs at 77.5 MHz or 62.0 MHz.

A.3 Crosstalk Worries

Crosstalk between the clock outputs from the LMK05318B can create spurs. The IC designers have addressed this by providing separate power supplies for each output driver. This worry is also mitigated by the attenuation provided by the LMX2572 that follows. However, they recommend:

> *"Separating clock outputs when the difference of the two frequencies, |fOUTx – fOUTy|, falls within the jitter integration bandwidth (12 kHz to 20 MHz, for example). Any outputs that are potential aggressors should be separated by at least four static pins (power pin, logic pin, or disabled output pins) to minimize potential coupling. If possible, separate these clocks by the placing them on opposite output banks, which are on opposite sides of the chip for best isolation." [LMK05318B datasheet]*

In our case, the difference frequencies between the reference clock outputs from the LMK05318B could be 38.0, 37.5, 22.5, 15.5, 15.0 or 0.5 MHz. Crosstalk issues will be greatly mitigated by the limited PLL bandwidth provided by the LMX2572 that follows in all cases except for the 0.5 MHz difference case. Because of this, if the LMK05318B is sourcing 62.5 MHz, then the 62.0 MHz option will be made unavailable.

A.4 LMX2572

The OSC input will be an output from the LMK05318B at submultiples of 2,500 MHz, or of 3,100 MHz, with the choice being made to avoid IBSs, as will be described.

The LMX2572 locks its 3.2 GHz to 6.4 GHz VCO to a multiple of the reference frequency input. The maximum phase detector frequency is about 100 MHz, which arises from the "Minimum N Divider Restrictions" shown in Table 3 of the datasheet. Knowing this, we will use LMK05318 output dividers large enough to create input reference frequencies of 100 MHz or less.

The output frequency from a clock synthesizer channel is given by:

$$f_{\text{out}} = \frac{f_{\text{APLL}} \cdot [INT + NUM/DENOM]}{D_{\text{LMK}} \cdot D_{\text{LMX}} \cdot D_{\text{FPGA}}}, \tag{A.1}$$

where f_{APLL} is either 2,500 MHz or 3,100 MHz, $N_{\text{divider}} = [INT+NUM/DENOM]$, D_{LMK} is the output divider on the LMK05318, D_{LMX} is the output divider on the LMX2572, and D_{FPGA} is the divider on the FPGA. There would be a factor of two in the numerator of the above expression if we were operating the LMX2572 in the "SYNC MODE", but we won't be (as it would cut the maximum f_{pd} in half, and we can accomplish phase alignment more accurately by other means).

A.5 Frequency Resolution

The frequency step size is given by:

$$\text{Frequency step size} \equiv \Delta f = \frac{d(f_{\text{out}})}{d(NUM)} = \frac{f_{\text{APLL}}}{D_{\text{LMK}} \cdot D_{\text{LMX}} \cdot D_{\text{FPGA}} \cdot DENOM}. \tag{A.2}$$

Small frequency steps are achieved by using a large value for *DENOM* and by incrementing the value of *NUM* by one. The 32-bit value of *DENOM* is programmable, and will be set so as to provide decimal frequency steps, Δf, of 0.1, 0.01, 0.001 Hz (and so on). *DENOM* must be a positive integer less than 2^{32}.

Solving Eq A.2 for *DENOM* we have:

$$DENOM = \frac{f_{APLL}/\Delta f}{D_{\text{LMK}} \cdot D_{\text{LMX}} \cdot D_{\text{FPGA}}} \tag{A.3}$$

With:

$$f_{\text{APLL1}} = 2,500,000,000 = 2^8 \cdot 5^{10}$$
$$f_{\text{APLL2}} = 3,100,000,000 = 31 \cdot 2^8 \cdot 5^8$$
$$1 \,/\, \Delta f = 10^N = 2^N \cdot 5^N \quad \text{where} \quad N = 1, 2, 3, \ldots$$

For *DENOM* to be an integer, the numerator of Eq A.3 must have matching prime factors to the denominator, which restricts the allowed values for D_{LMK}, D_{LMX}, and D_{FPGA}. All this can work out with the given values of D_{LMX} $(1, 2, 4, 8, \ldots, 256)$ and by using values of D_{LMK} and D_{FPGA} which only have prime factors of 2 and 5.

As an example, suppose we want to generate a clock output of exactly 1 MHz with 0.00001 Hz resolution. Using f_{APLL} of 2.5 GHz, a D_{LMK} of 25, D_{LMX} of 256, and D_{FPGA} of 20 we have:

$$DENOM = \frac{f_{\text{APLL}}/\Delta f}{D_{\text{LMK}} \cdot D_{\text{LMX}} \cdot D_{\text{FPGA}}} = \frac{(2^8 \cdot 5^1 0) \cdot (2^5 \cdot 5^5)}{5^2 \cdot 2^8 \cdot (2^2 \cdot 5)} = 2^3 \cdot 5^{12} = 1,953,125,000.$$

We can find the required $N_{\text{divider}} = [INT + NUM \,/\, DENOM]$ by rearranging Eq A.1:

$$N_{\text{divider}} = \frac{f_{\text{out}} \cdot D_{\text{LMK}} \cdot D_{\text{LMX}} \cdot D_{\text{FPGA}}}{f_{\text{APLL}}} = \frac{1,000,000 \cdot 25 \cdot 256 \cdot 20}{2,500,000,000} = 51.2. \tag{A.4}$$

A.6 Avoiding Integer Boundary Spurs

Considering only the top octave for the LMX2572 (3.2 GHz to 6.4 GHz), with an input reference frequency of 100 MHz, the integer part of the N-Divider will be between 32 and 64. Inherently, the required N-divider will approach an integer boundary whenever the requested output frequency approaches a harmonic, or sub-harmonic, of the input reference frequency. We can avoid this by changing the output divider on the LMK05318, or by switching between APLL1 and APLL2.

A pathological case illustrates the need for APLL2. If the requested frequency is very close to 5 GHz, the N-divider for the LMX2572 will be very close to twice the output channel divider used on the LMK05318B, which would generate a large IBS. (A similar situation happens for output frequencies of 3,750 MHz and 6,250 MHz that illustrate both IBSs and ½-IBSs.) We can move away from the IBS by selecting APLL2, whose operating frequency is not harmonically related to that of APLL1.

Any scheme to avoid IBSs must be compatible with the restrictions of decimal frequency steps detailed above. While the solution is difficult to 'derive', the outcome is not complicated. We can avoid IBSs and get decimal frequency steps by choosing between four reference frequencies to the LMX2572. The four choices are f_{APLL1} / 25, f_{APLL1} / 40, f_{APLL2} / 40, and f_{APLL2} / 50 which provide f_{pd} frequencies of 100.0 MHz, 62.5 MHz, 77.5 MHz or 62.0 MHz to the LMX2572. (Notice that the divisors, 25, 40 and 50 have only prime factors of 2 and 5.)

How should the instrument's firmware choose between these four alternatives? How close to an integer boundary, or half-integer boundary, is too close? And will this scheme work for any frequency?

To make the choice, the firmware will evaluate the figure of merit (FOM) for the four options and choose the best one. We should also consider that selecting a new reference frequency, and computing and loading new a new N_{divider}, will disrupt the phase of the clock output. In order to minimize these events, and to allow small steps around any frequency without recurring disruptions, we will only change between alternatives if the new FOM is at least 10% better than the current FOM. Doing so will provide hysteresis band between the switchovers.

(We will use a similar strategy to avoid disruptions as the user tunes across the LMX2572's octave boundaries. This will be done by allowing the LMX2572 to be tuned by about 1% beyond its octave boundary before switching to the new octave. The 2% hysteresis band will eliminate recurring disruptions for small frequency steps at octave boundaries.)

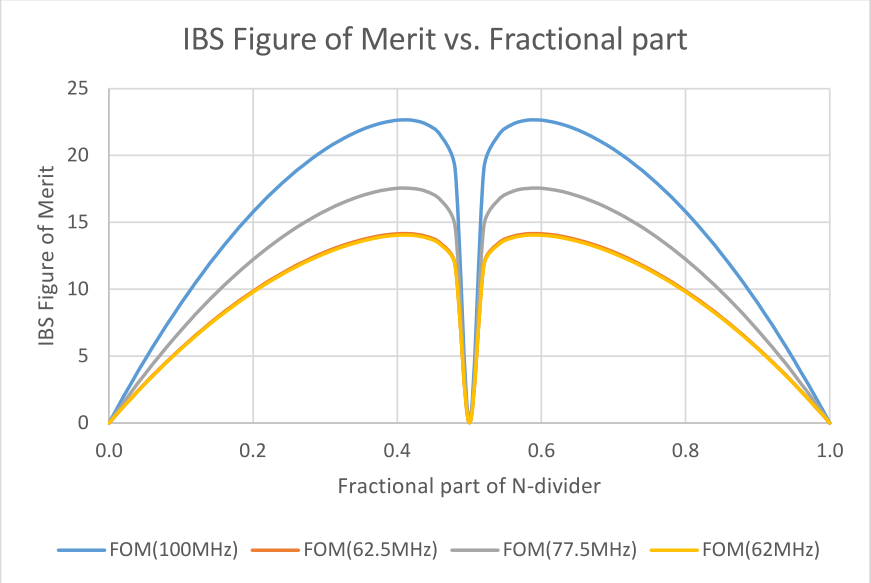
A.7 IBS Figure of Merit Function

The FOM function is an ad hoc estimator to evaluate the four reference frequency alternatives. The FOM provides a 'score'. The higher the score, the more favorable the alternative. The function is linear in the reference frequency, $f_{pd} = f_{APLL}/D_{LMK}$ (high values reduce broadband phase noise), is made smaller around integer boundaries, and is also made smaller very close to half-integer boundaries. Here it is:

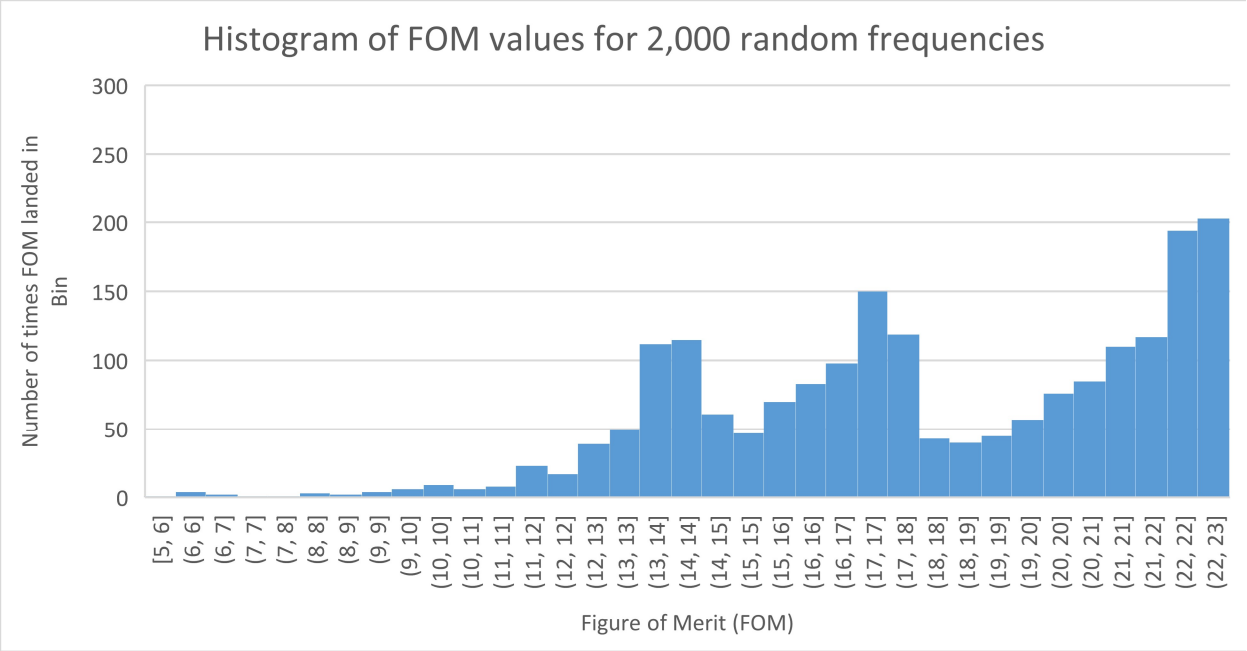
$$\text{Figure of Merit, FOM} = \frac{f_{pd}(\text{MHz})}{\frac{1}{n+\delta} + \frac{1}{1-n+\delta} + \frac{k}{|n-0.5|+\delta}}$$

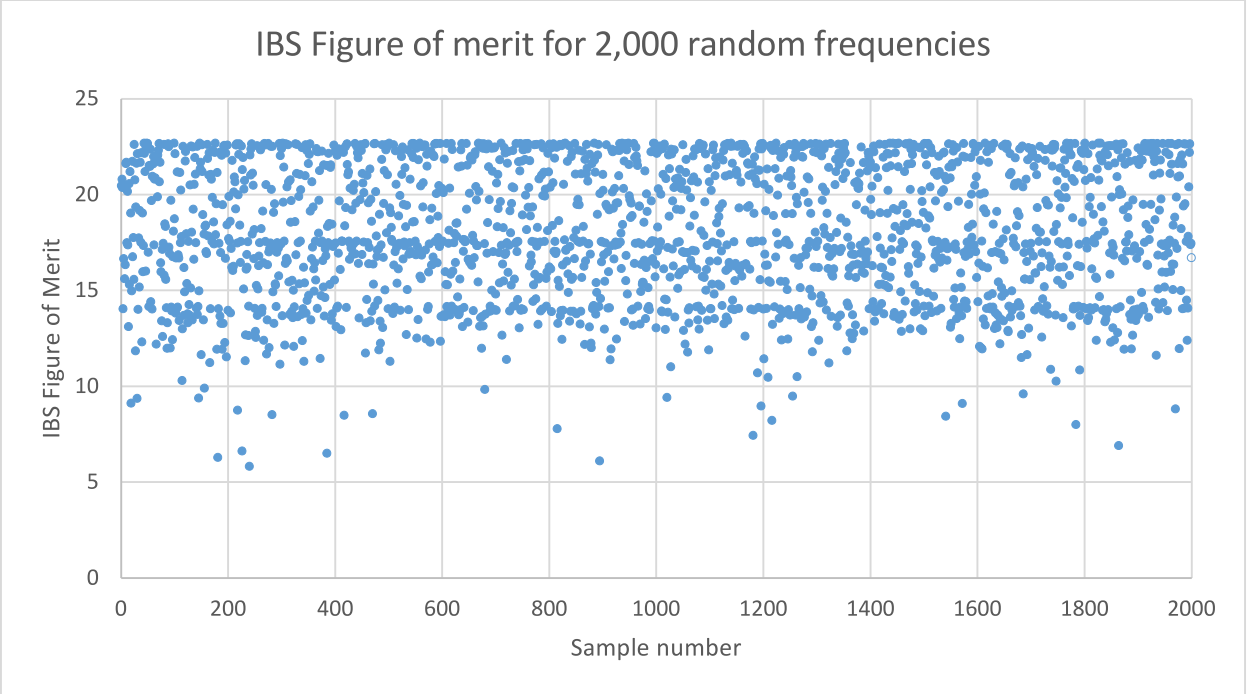
Here, n is the fractional part of the $N_{divider}$ and δ avoids singularities (a value of 1E-6 was used in the results shown below). The weighting factor for half-integer, vs. integer boundary spurs, k, is typically 0.025 (a weighting suggested in a TI App Note).

The IBS FOM function looks like this:



A spreadsheet was used to answer the question "Will this work at every frequency?" The spreadsheet computes the FOM for 2,000 random frequencies over the top octave of the LMX2572 and creates a scatter plot and histogram of FOM results. Below are typical results:





The average FOM for this data was 18.0 and the worst-case point had a FOM value of 5.7. Using the FOM functional curve, the worst-case point corresponds to a fractional N-divider of about 0.05, while the average result corresponds to about 0.25. Striations in data at FOM values around 24, 17 and 14 correspond to the lobe peaks in the IBS FOM estimator for

D_{LMX}	D_{FPGA}	Max f_{out}	Min f_{out}	Res (Hz)	DENOM	DENOM	DENOM	DENOM	HR
1	1	6,400,000,000	3,200,000,000	0.1	1,000,000,000	625,000,000	775,000,000	620,000,000	4.29
2	1	3,200,000,000	1,600,000,000	0.1	500,000,000	312,500,000	387,500,000	310,000,000	8.59
4	1	1,600,000,000	800,000,000	0.01	2,500,000,000	1,562,500,000	1,937,500,000	1,550,000,000	1.72
8	1	800,000,000	400,000,000	0.01	1,250,000,000	781,250,000	968,750,000	775,000,000	3.44
16	1	400,000,000	200,000,000	0.01	625,000,000	390,625,000	484,375,000	387,500,000	6.87
32	1	200,000,000	100,000,000	0.001	3,125,000,000	1,953,125,000	2,421,875,000	1,937,500,000	1.37
64	1	100,000,000	50,000,000	0.001	1,562,500,000	976,562,500	1,210,937,500	968,750,000	2.75
128	1	50,000,000	25,000,000	0.001	781,250,000	488,281,250	605,468,750	484,375,000	5.50
256	1	25,000,000	12,500,000	0.0001	3,906,250,000	2,441,406,250	3,027,343,750	2,421,875,000	1.10
256	2	12,500,000.00	6,250,000.00	1.00E-04	1,953,125,000	1,220,703,125	1,513,671,875	1,210,937,500	2.20
128	5	10,000,000.00	5,000,000.00	1.00E-04	1,562,500,000	976,562,500	1,210,937,500	968,750,000	2.75
256	5	5,000,000.00	2,500,000.00	1.00E-04	781,250,000	488,281,250	605,468,750	484,375,000	5.50
256	10	2,500,000.00	1,250,000.00	1.00E-05	3,906,250,000	2,441,406,250	3,027,343,750	2,421,875,000	1.10
256	20	1,250,000.00	625,000.00	1.00E-05	1,953,125,000	1,220,703,125	1,513,671,875	1,210,937,500	2.20
128	50	1,000,000.00	500,000.00	1.00E-05	1,562,500,000	976,562,500	1,210,937,500	968,750,000	2.75
256	50	500,000.00	250,000.00	1.00E-05	781,250,000	488,281,250	605,468,750	484,375,000	5.50
256	100	250,000.00	125,000.00	1.00E-06	3,906,250,000	2,441,406,250	3,027,343,750	2,421,875,000	1.10
256	200	125,000.00	62,500.00	1.00E-06	1,953,125,000	1,220,703,125	1,513,671,875	1,210,937,500	2.20
128	500	100,000.00	50,000.00	1.00E-06	1,562,500,000	976,562,500	1,210,937,500	968,750,000	2.75
256	500	50,000.00	25,000.00	1.00E-06	781,250,000	488,281,250	605,468,750	484,375,000	5.50
256	1,000	25,000.00	12,500.00	1.00E-07	3,906,250,000	2,441,406,250	3,027,343,750	2,421,875,000	1.10
256	2,000	12,500.00	6,250.00	1.00E-07	1,953,125,000	1,220,703,125	1,513,671,875	1,210,937,500	2.20
128	5E+12	1.00E-05	5.00E-06	1.00E-16	1,562,500,000	976,562,500	1,210,937,500	968,750,000	2.75
256	5E+12	5.00E-06	2.50E-06	1.00E-16	781,250,000	488,281,250	605,468,750	484,375,000	5.50
256	1E+13	2.50E-06	1.25E-06	1.00E-17	3,906,250,000	2,441,406,250	3,027,343,750	2,421,875,000	1.10
256	2E+13	1.25E-06	6.25E-07	1.00E-17	1,953,125,000	1,220,703,125	1,513,671,875	1,210,937,500	2.20

Table A.1: Dividers used to generate any frequency from 1 μHz to 6.4 GHz

f_pd values of 100 MHz, 77.5 MHz and 62.5 MHz. All the results are far enough away from integer, and half-integer, boundaries to effectively remove IBSs as a pragmatic concern.

A.8 Operational Details

Table A.1 shows the sequence of dividers used to generate any frequency from 1 μHz to 6.4 GHz. Given a desired output clock frequency, the IBS FOM will be used to select the best PLL frequency and output divider on the LMK05318B, thereby selecting one of the four columns of DENOM values.

It would be nice if we could just use binary division in the FPGA. Unfortunately, doing so will not support decimal resolution steps, and so we must also divide by 5. Whenever a new divide-by-5 stage is used in the FPGA, we need to reduce the LMX2572 output divisor from 256 to 128, which creates overlapping frequency bands.

"HR" (headroom) is equal to $2^{32}/DENOM$. We want the largest integer DENOM that will provide decimal resolution (bigger is better) but

DENOM must be less than 2^{32} (about 4.29E+9). Headroom is also a measure of wasted resolution. The decimal frequency resolution is selected so that the Headroom is a number between 1 and 10.

A.9 Enabling Integer-N

We went to a great deal of effort to avoid operating nearby integer-N values. Doing so assured that the clock outputs would not be plagued by IBSs, and that we could tune seamlessly across any small frequency range.

However, there may be circumstances in which user will want to operate in the integer-n mode. Doing so will provide the lowest phase noise clock outputs at common decimal frequencies.

For example, suppose a user wants a very clean 1 GHz clock. It is most likely that the very best performance could be achieved using a frequency reference input from the LMK05318B of 100 MHz, operating the LMX2572 at exactly 4 GHz by using a N-divider value of 40, and dividing the LMX2572LP output by 4.

With this we should consider a GUI feature to "Enable Integer-N", in which case the IBS FOM search would allow integer-N solutions. In that case, if the user attempted to make a small frequency step away from the integer-N value, they would be warned that the "Enable Integer-N" mode would be turned off before the step could be made.

A.10 Phase Adjustments

Currently, the hardware supports the ability to measure the phase between two LMX2572 RF outputs which are operating at the same frequency. (It is possible that we will be able to adjust the phase of harmonically related clocks, subject to certain restrictions.) The current phase detector design is very good at finding quadrature (90° phase between the two LMX2572s). From there, we could dead reckon to the desired phase. There are at least three ways to adjust the phase of the LMX2572 outputs.

The first phase adjustment method is done by writing to the MASH_SEED register. Unfortunately, doing so can only add phase delay (writes to MASH_SEED can not advance the phase). Phase adjustment by writing MASH_SEED is possible with integer channels (PLL_NUM = 0) as long as MASH_ORDER is greater than 1. This technique adjusts the phase of the VCO. The phase shift of the output will be less by a factor equal to $D_{\text{LMX}} \cdot D_{\text{FPGA}}$, which could require billions of MASH_SEED writes to adjust the phase of a 1 Hz output.

We can also adjust the phase by running off frequency for a deterministic time interval. Doing so can provide both positive and negative phase adjustments. The frequency shift should be small to avoid requiring a VCO recalibration, and in the case that we are at an octave boundary of the VCO. (We could create overlapping frequency bands, and so avoid the VCO's octave boundaries, by creative modifications to the FGPA sequence detailed in the table above.)

Finally, we can adjust phase of low frequency clocks (<50 MHz) by shortening, or extending, the FPGA divider count. We will need to implement this method to speed up phase adjustments at low frequencies. For example, 1 Hz clock could be generated by dividing a 20 MHz output from an LMX2572 by 20,000,000. Suppose that we want to adjust the phase of the 1 Hz output by 90°. The RF VCO tuning limitations mentioned above may limit the frequency shift to just 1% of the VCO frequency. With that, it would take 25 seconds to move the phase by 90°. A faster way to advance the phase by 90° would be to divide the 20 MHz signal by 15,000,000 just once, and then return to dividing by 20,000,000 thereafter. To retard the phase by 90° we would divide the 20 MHz signal by 25,000,000 just once and then return to dividing by 20,000,000. Doing so, the phase adjustment would be done in a single cycle.

A.11 Modulation Capability

The CG792 clock generators have analog and digital inputs, via rear panel BNCs, for blanking and frequency and phase modulation (FM and PM). The digital input has a threshold at 1 V (for 3.3 V logic). The analog input has a range of ± 1.00 Vdc. Both inputs have a 1 MΩ input impedance.

All clock channels use an LMX2572 RF frequency synthesizer. While digital blanking is done after the synthesizer (at the output drivers), all frequency and phase modulation is done in the LMX2572 via its SPI port. The SPI port is connected to the small FPGA which is also on the clock channel card.

The LMX2572 was designed to operate with low phase noise at a fixed frequency, or, over a small range of frequencies. Low phase noise was facilitated by splitting the octave tuning range (3.2 GHz to 6.6 GHz) of the VCO into six smaller frequency bands, shown in Table 136 of LMX2572 datasheet.

The 32-bit programmable denominator (for the fractional part of the N-divider) provides high resolution, decimal friendly, frequency steps. Typically, whenever a new frequency is set, the VCO will be "calibrated". Calibration can require more than 100 μs, and will totally disrupt the phase of the RF output from the part. Clearly, VCO calibration during FM or PM must not happen.

We can avoid the disruption of VCO calibration by limiting the modulation frequency deviation. Doing so will place a limit on the FM deviation, and will limit the PM slew rate. Unfortunately, the six VCO bands are not overlapping, and so when operating on a boundary between two bands we have to hope for the best. The specification sheet for the part (in the description of the ramping function) suggests that if the ramp range is less than 10 MHz, no VCO calibration will be required. (This is certainly true in the center of any of the VCO bands.) At the lowest VCO frequency, 10 MHz corresponds to a 0.3125 % deviation (or 3,125 ppm). We will use this fractional frequency deviation to set a safe upper limit for the FM deviation.

A.12 Analog FM

The analog modulation input has a range of ± 1.00 V and its bandwidth is limited to 35 kHz (yielding 10 µs transition times). The bandwidth limited signal is sampled at 1 Msps.

The instantaneous frequency of the clock output will be given by:

$$f(t) = [1 + \delta \cdot v_{\mathrm{mod}}(t)] \cdot f_0$$

Where f_0 is the frequency of the unmodulated clock, $v_{\mathrm{mod}}(t)$ is the applied analog modulation voltage, and δ is the fractional frequency deviation scale factor, whose values will be selected from the 1–2–5 sequence of 0.002, 0.001, 0.0005, 0.0002, 0.0001, ..., 10^{-12} (with units of V^{-1}).

The 2,000 ppm upper limit for δ will allow the clock generator to cover the worst-case error for crystal oscillators, and the lower limit will allow clock steering well below the stability of the best commercial frequency sources. Unfortunately, that maximum frequency deviation will also limit the maximum phase slew rate as we shall see next.

A.13 Analog PM

We cannot directly control the phase of the LMX2572's RF output, rather, we can slew the phase to a new value by offsetting the clock frequency for a known period of time. The phase shift, $\Delta\phi$, from a frequency offset, Δf, for a fixed interval, Δt, is given by

$$\Delta\phi \text{ (radians)} = 2\pi \cdot \Delta f \text{ (Hz)} \cdot \Delta t$$

The accumulated phase from a series of frequency offsets over N intervals is given by

$$\phi_N = \phi_{\mathrm{start}} + \sum_{i=1}^{N} \Delta\phi_i = 2\pi \cdot \Delta t \cdot \sum_{i=1}^{N} \Delta f_i$$

The user will be able to control the phase via the external analog modulation input. The gain for this input is β (rad/V). We want the accumulated phase to equal the requested phase to null the error.

$$\phi_{\text{error}} = \beta \cdot v_{\text{mod}}(t) - 2\pi \cdot \Delta t \cdot \sum_{i=1}^{N} \Delta f_i$$

With that, the best guess for the Δ◎ in the next time interval is given by

$$\Delta f_{N+1} = \frac{\phi_{\text{error}}}{2\pi \cdot \Delta t} = \frac{\beta \cdot v_{\text{mod}}(t)}{2\pi \cdot \Delta t} - \sum_{i=1}^{N} \Delta f_i$$

There is an important restriction on this result: $|\Delta f|$ must be less than the maximum allowed frequency deviation (about 3,125 ppm of d_0 as described above). If the allowed Δf is less than what is needed to null the phase error, and so track the PM input, then deficit will be saved up for future intervals. The limited phase slew rate may be noticeable to users.

The maximum phase slew rate is given by

$$\text{Max phase slew rate} = \frac{\Delta\phi_{\text{max}}}{\Delta t} = 2\pi \cdot \Delta f_{\text{max}}$$

And so, the time required to make a phase step, $\Delta\phi$, is given by

$$\Delta t = \frac{\Delta\phi}{2\pi \cdot \Delta f_{\text{max}}}$$

Suppose, for example, that the user requests a $\pi/2$ (90°) phase step on a 1 kHz clock. With the largest allowed frequency shift of 3,125 ppm of 1 kHz (3.125 Hz), the time required to slew to the correct phase is given by

$$\Delta t = \frac{\Delta\phi}{2\pi \cdot \Delta f_{\text{max}}} = \frac{\pi/2}{2\pi \cdot 3.125} = 0.080\,\text{s}$$

So, it would require 80 cycles of the 1 kHz clock for the phase to slew by 90° (which is a lot longer than the 10 µs risetime of the bandwidth limited analog modulation input). Note that a 1° phase shift could be accomplished during a single clock cycle of the 1 kHz clock. Note also that a 90° phase of a 100 MHz clock could be done 100,000 times faster (or in 0.8 µs). However, the phase slew rate in that case would be limited by the 10 µs risetime of the LPF on the analog modulation input.

A.14 Phase Drift

There are some computational challenges, and hardware uncertainties, that may cause the phase to drift when using the analog modulation input.

The computational challenge will be to eliminate sources of error in the FPGA's phase accumulator which is keeping the sum of Δf's. Hopefully, the integer nature of the LMX2572's N-divider will make it possible to avoid any rounding errors in the sum. What other error sources might exist?

The principal hardware uncertainty is the behavior of the LMX2572 when it's told (via the SPI) to change frequency (via the N-divider). The question is, "If the LMX2572 is told to step up in frequency by a Δf for some period of time, then told to step down in frequency by the same Δf for same period of time, will there be any phase error?" This, of course, will depend on the exact timing used by the LMX2572 to initiate the frequency steps. To give us a fighting chance, the FPGA uses the same clock as the LMX2572, on the hope that the timing of those events will be exactly the same.

Appendix B Circuit Description

This appendix provides an overview of the circuit of the CG792 Multichannel Clock Synthesizer. The description refers to the schematic sheets included at the end of this manual.

In the circuit descriptions which follow, net pairs which are named (for example) REF_CLK_P and REF_CLK_N on the schematics, will be renamed ±REF_CLK in the text description.

B.1 Synthesizer and FPGA

See Clock channel card, Sheet 2 of 3.

Each clock channel (two on the front panel, and up to two as rear panel options) consists of an RF synthesizer (U106, an LMX2572), a small FPGA (U113), and high-speed output drivers (on Sheet 2 of 2). Connections to the motherboard, via the vertical PCB, appear on P100.

Each clock channel card has its own frequency synthesizer and high-speed output drivers. Single-ended CMOS clock levels (DC to 250 MHz with sub-ns transition times), and differential clock outputs (DC to 2.2 GHz with about 40 ps transition times) are provided on BNCs.

There is a small vertical PCB which can connect one or two clock channels, mounted on either the front or rear panel, to the motherboard.

Each RF synthesizer has its own reference frequency, ±REF_CLK (between 62 MHz and 100 MHz and sourced from the motherboard). The RF synthesizer is initialized and controlled by the FPGA. The synthesizer has a wideband VCO and a fraction-N PLL synthesizer, to provide outputs from 12.5 MHz to 2.2 GHz (for the LMX2572LP).

There are two differential RF outputs from the synthesizer. The ±RF_A output is only used for frequencies above 2.2 GHz (in the CG796), and so is provided a direct path to the output drivers via ±UHF_OUT. The ±RF_B outputs drive the input of a 1:4 LVPECL fanout (U109). Outputs from the fanout allow phase measurement on the motherboard (via ±PHASE_OUT), serve as the clock output source for clocks between 12.5 MHz and 2.2 GHz (via ±HF_CLK1), drive the FPGA's divider input (via ±HF_CLK3). The FPGA's divided output is re-sync'd to the reference clock by ±HF_CLK2 and U110.

A high-speed differential multiplexer (U108) is used to select between the undivided RF output (±HF_CLK1), and the divided (and re-sync'd) FPGA output (±RSYNC), as the source for the channel output drivers. The multiplexer output drives another 1:4 LVPECL fanout to provide sources for the differential output drivers (±DIFF_OUT), the CMOS output drivers (±CMOS_OUT), and the channel synchronization circuits (±CLK2_OUT). Note that unselected LVPECL outputs will become inactive (and float high) as there is no emitter current being drawn.

The clock sources (±DIFF_OUT and ±CMOS_OUT) can be set to a fixed blanking level as determined by the BLANK_POL bit. Blanking logic (U100, U101, U104 & U105) can be asserted asynchronously by the

MPU (via U102) or via the external digital modulation input (with EXT_BLANK_EN asserted). Firmware will always disable the CMOS output for frequencies above 250 MHz.

The ±PHASE_OUT and ±CLK2_OUT signals are connected to the phase measurement and channel synchronization circuits on the motherboard via a high-speed SATA cable via P101. SATA cables provide two high-speed differential pairs with 100 Ω differential impedance.

The FPGA uses the same reference clock as the RF synthesizer, and is controlled by the MPU on the motherboard. After initializing the RF synthesizer, the FPGA can be used to provide divided clock outputs below 12.5 MHz. The FPGA can also adjust, or modulate, the frequency and phase of the synthesizer via the RF synthesizer's SPI interface.

An FPGA_SYNC is asserted by the motherboard when the user requests phase synchronization between two or more channels. That signal can be used to restart the divide-by-N counters in the FPGA, and, if EN_LMX_SYNC is set high, will also assert the SYNC input to the LMX2572. (The SYNC pin can be used to establish a deterministic phase relationship between the OSCin and RFout. There are many restrictions on its use, and it probably will not be used, as the LMX2572 phase is adjusted by other means.)

B.2 Output Driver

See Clock channel card, Sheet 3 of 3.

Each clock channel has three outputs on either BNCs (for DC to 2.2 GHz). The MPU is able to monitor the divided voltage at each output via CMOS_MON, and ±CLK_MON.

One output provides a single-ended, +3.3 V CMOS clock from DC to 250 MHz, via a 50 Ω source impedance. This output has a 1 ns transition time, and is intended to drive high impedance loads to +3.3 V, while reverse terminating the reflected wave. (The output can also drive 50 Ω loads, to +1.65 V, for which there is no reflected wave.)

The CMOS output driver consists of gang of four LVDS to CMOS line receivers (U200). The CMOS outputs from these devices has a typical source impedance of 20-30 Ω. Placing a 174 Ω resistor in series with each output, provides a source resistance of about 200 Ω. Placing four in parallel yields a source resistance close to 50 Ω.

The LVDS line receivers typically show substantial overshoot on their outputs, especially when all the gates on a die transition simultaneously. This artifact is reduced by implementing a snubber on the part's Vcc (instead of just the usual bypass capacitor). Here, R202, a 4.7 Ω resistor

serves the purpose, inserting loss in series with the part's Vcc bond wire, to provide a much cleaner clock output waveform.

The remaining two outputs provide a differential clock, with less than 50 ps transition times, into 50 Ω loads. The outputs are compatible with virtually every differential logic level (ECL, LVDS, PECL, LVPECL, CML, etc.), with output amplitudes from 0.1 Vpp to 1.2 Vpp and common mode voltages ranging from 3.0 Vdc to +2.0 Vdc. (The user can specify the amplitude, Vpp, and common mode voltage, Vcm, for the differential outputs via the front panel GUI.)

A key component for the high-speed differential outputs is U203, a ONET4211LD laser diode driver (LDD). The part provides a switchable current source, programmable from 5 to 85 mA, with typical 35 ps rise and fall times, and a typical random jitter of 600 fs. The part is designed to operate from a +3.3 Vdc supply. The principal difficulty of using this part is its limited compliance range of its current outputs, which is between +0.6 V and +4.8 V, or a common mode range which is centered +2.7 V above the part's ground reference. Further, the current output drivers for the part require a 20 Ω load.

To meet all of these requirements, the LDD is operated from dual tracking power supplies, separated by +3.3 Vdc. The "GND" reference to the part is provided by an adjustable negative voltage regulator, U208, (it has to sink current, after all), controlled by an 8-bit DAC, U207, for "GND" references between +0.1 V and -6.9 V. (The required "GND" reference voltage will depend on the user specified Vpp and Vcm.) The "VCC" for the LDD is provided by a fixed +3.3 V regulator, U205, which is referenced to the part's "GND" reference.

The ±MOD outputs from the LDD see a load of 30.1 Ω (R223 or R224), in parallel with 70 Ω (R225 or R226 in series with the user's 50 Ω loads), or about 21 Ω in total. While this closely matches the required load, in also means that only about 30 % of the switched current output from the LDD appears in the user's load, with the balance passing through R223 and R224.

The 30.1 Ω resistors are pulled up with a programmable voltage source (U201) to provide the user requested common mode output voltage. The output of the buffer amplifier will set to 2*VCM+VPP, or between -5.9 V and +5.2 V. The input to the buffer amplifier, from U202B, provides a gain of x5 for the OFFS_CTL from another 8-bit DAC channel.

The amplitude of the outputs is proportional to the ±MOD current, which is programmed by the current drawn from the MODSET pin on the LDD. In TI suggested designs, the MODSET current is set with a resistor between the MODSET pin and ground. The data sheet notes the maximum ±MOD current of 85 mA is achieved with a resistor of 3.1 kΩ. TI does not specify the potential at the MODSET pin; typically, it would

be +1.2 Vdc above the LDD's ground, for which the MODSET current would be 387 μA. In the current design, the 8-bit DAC is able to program MODSET current between 0 and 500 μA, using a 4.99 kΩ resistor (R238) to the virtual null at the non-inverting input to the op amp, U206A. The current mirror, Q205A and Q205B, provides the inverted dc feedback to the op amp and draws an equal current from the MODSET pin on the LDD.

The clock input to the LDD needs to be level shifted to tract the LDD ground reference which is adjusted to meet the user-requested common mode output voltage. The level shifting must be done without damaging the differential signal's very high bandwidth. There are two cases. High frequency clock outputs can simply be ac coupled (unless the clock is stopped). Low frequency clocks will require true level shifting, with proper dc restoration. (Low frequency clocks are always sourced via the ±DIFF_OUT differential pair.)

A high bandwidth analog multiplexer, U204, is used to select between the ±UHF_OUT and ±DIFF_OUT differential pairs. In the case of the ±UHF_OUT pair being selected, the signal is coupled to the LDD through C211 and C213 and the dc restoration current sources, Q200 & Q201, are turned off.

In the case of the ±DIFF_OUT pair being selected (for frequencies < 2.2 GHz or when the clock is turned off and set to a fixed level), the high frequency components of the clock are again coupled via C211 and C213, while the low frequency components (<50 MHz as set by L203/L204 and R233/R234) pass though the differential PNP/NPN cascode pair, Q203/Q204 & Q200/Q201. The dc-restoration cascode outputs are enabled by -DC_RESTORE going low which turns on each of Q200/Q201 with about 22 mA of dc current.

The output polarity of the LDD can be controlled with the OUTPOL input on the LDD. The control for this, DIFF_POLARITY, is sourced by the FPGA and needs to be level shifted to track the LDD's floating power supplies. High frequency components of that control signal are passed directly to the LDD via C212, and the dc restoration is done by the differential amplifier, U202A, which sums the LDD's ground to the polarity control signal to bias the OUTPOL input to the LDD.

B.3 Connecting Clock Channels to Motherboard

See Vertical PCBs, Sheet 1 of 1.

The motherboard provides power, reference clocks, and data interfaces to the clock channel cards. There are two clock channel cards mounted on the front panel, and up to two on the rear panel. The clock channel

cards connect to the motherboard via a small vertical PCB with three 30-pin connectors.

The data interface consists of a bi-directional SPI port with two port selects (CS_SR and CS_ETC). The CS_SR latches 8-bits into a serial-in, parallel-out shift register, U2. The latched bits are used to fanout the CS_ETC to one of six SPI devices on the clock channel cards, or to select one of eight analog signals for measurement by the MPU on the motherboard.

The FPGAs on the clock channel cards require power supply sequencing on power-up. Two power switches, U6 and U8, delay the +3.3V and +2.5V power supplies for about 100 ms after the +3.3V power has settled.

High speed multiplexers on the clock channel cards require offset power supplies to allow them to multiplex LVPECL level logic signals. low-current power supplies at +4.3 V and +1.0 V are provided by the dual op amp, U5. The op amp circuits are designed to be stable even with the 1 μF bypass capacitor on the power supply output.

A 1:8 analog multiplexer, U4, allows the MPU on the motherboard to measure the analog voltage on any of the six outputs from two clock channel cards. The MPU can also measure the power supplies for the high-speed multiplexers.

An LVDS line receiver terminates and converts the differential ±EXT_MARK signal to a single-ended signal that is sent to each clock channel card.

B.4 Timing References

See Motherboard, Sheet 1 of 4.

All system frequencies are sourced by U102, an LMK05318B frequency synthesizer. The LMK05318B is controlled by the MPU via a (mostly quiet) SPI interface.

The LMK05318B has two APLLs. Both APLLs have low phase noise. APLL1 has a narrow band 2,500 MHz BAW VCO with very low phase noise. This VCO will be locked to the 24.576 MHz TCXO input using an N-value of about 101.725260, nicely away from integer and half-integer boundaries, thereby avoiding integer boundary spurs (IBSs). The VCO is phase locked to the TCXO with a loop bandwidth of about 10 kHz.

There is another, much slower, DPLL which is used to phase lock APLL1's 2.5 GHz VCO to a 10 MHz reference (the OCXO, rubidium, or external 10 MHz frequency references) When enabled, the TCXO frequency is left free-running, but the fractional part of the 101.725260 N-divider is adjusted to keep the VCO phase locked to the 10 MHz reference. Doing so corrects for the aging, drift and low frequency phase noise of the TCXO. The DPLL operates with about 4 kHz bandwidth.

The second APLL is used to avoid IBSs in the case that the divided outputs from APLL1 cannot do so. The reference frequency to APLL2 will be 100 MHz, sourced from APLL1 by dividing its 2.5 GHz VCO with RP=5 and RS=5. APLL2 will be locked to 6,200 MHz, just below its top operating frequency of 6,250 MHz, by using an integer divider of 62. The APLL2 bandwidth is about 1 MHz.

Outputs from the LMK05318 are low jitter, 100 Ω, differential logic clocks at up to six different frequencies between 10 MHz and 100 MHz. The VCO output is divided by 250 to provide 10 MHz outputs on OUT0 and OUT1 for the rear panel 10 MHz outputs. The output divider is set to 50 to provide 50 MHz outputs on OUT2 and OUT3 for the MPU and motherboard FPGA clock inputs. The output divider will be set to either 25 or 40 to provide clock channel reference frequencies of 100 MHz or 62.5 MHz. Finally, the post-divider for APLL2 output will be set to 2, and the output divider will be set to 40 or 50, to provide clock channel reference frequencies of 77.5 MHz or 62.0 MHz.

B.5 10 MHz Timebase References

As described above, the LMK05318B locks its VCOs to the 24.576 MHz TCXO input, and uses a DPLL, with a 10 MHz reference frequency, to trim the frequency offset and drift of the TCXO. There are two possible sources for the DPLL's 10 MHz reference: ±PRIREF and ±SECREF. The primary reference is the rear panel external 10 MHz input, which will always be given priority. The secondary reference is provided by either the optional OCXO, or by the optional rubidium frequency standard. The secondary reference will be used if either option is installed and warmed up, provided that the rear panel external 10 MHz is not present.

The external 10 MHz reference input is both ac (C114) and transformer (T100) coupled, with a nominal input impedance of 50 Ω at 10 MHz. The user-supplied input should be a sinewave between 1 and 3 Vpp. Typically, the input reference frequency error is well below 1 ppm. The single-ended 10 MHz input is converted to a differential 10 MHz output, with a common-mode voltage of +1.65 V, that is discriminated by a fast comparator (U101), which provides a 10 MHz PRIREF to the LMK05318B.

The 10 MHz references from either the OCXO or rubidium frequency standard are also transformer (T102) coupled. The single-ended 10 MHz input is converted to a differential 10 MHz output, with a common-mode voltage of +1.65 V, that is discriminated by a fast comparator (U105), which provides a 10 MHz SECREF to the LMK05318B.

There are two 10 MHz timebase reference outputs from the LMK05318B. Each of the outputs are at HCSL levels (differential 15 mA current sources intended to drive 50 Ω ground-referenced loads). The outputs

are amplified by low-noise, common-base, differential amplifiers (Q100-Q103), converted to single-ended outputs (by T101 and T103), low-pass filtered, and output on the rear panel on BNC connectors. The outputs, which have a nominal 50 Ω output impedance, can drive 50 Ω loads to ground with about 2 Vpp, and have very high isolation between them. The LPFs have a notch at 30 MHz, and do a very good job of converting the 10 MHz HCSL square wave outputs into clean sinewaves.

B.6 Modulation Inputs

There are two rear-panel modulation inputs. These inputs allow the user to modulate the frequency or phase of selected clock channel outputs. Both inputs have a 1 MΩ input impedance to ground.

The digital input, which has a positive-going switching threshold of +1.00 Vdc and 160 mV of hysteresis, can be used for both FSK and PSK (frequency and phase-shift keying) and blanking (forcing a clock output to a fixed level). The digital input is protected by R129, discriminated by the comparator U111, which in turn drives U110, to provide two LVDS pairs (one each for the front and rear panel vertical PCBs and clock channel output drivers). The discriminated output, EXT_MARK, is also provided to the motherboard's modulation FPGA.

The analog modulation input is buffered and amplified by U115A, which drives the input of a two-stage, forth-order, Bessel low-pass filter with a -3 dB bandwidth of 35 kHz which limits the input slew rate to 10 μs. The final stage of the LPF, U114, provides differential outputs to drive the input of a 1 Msps, 14-bit ADC. The over-all, differential, front end gain is x2.00. (A 1.00 Vdc input will generate a 2.00 Vdc difference between the differential outputs.) The common mode output voltage is +1.50 Vdc.

The ADC is connected via an SPI to the motherboard's FPGA. That FPGA can re-frame the ADC data and provide modulation data streams to the front and rear vertical PCBs, allowing the modulation data to be streamed to any of the four clock channels.

The analog modulation input can also be used as a general-purpose ADC input using ±MOD_IN and the MPU's ADC.

The FPGA requires power-up sequencing, with the +1.2 V core logic supply turning on first, followed by the +3.3 V and +2.5 V supplies, which are supplied via U107 and U109 after the system -RESET is released. The FPGA is clocked by a 50 MHz differential signal (±MB_FPGA_CLK) from the LMK05318B. This clock is divided by the FPGA to provide either a 25 MHz or 1 MHz clock to the front panel GUI. Doing so synchronizes the GUI to the main timebase, thereby avoiding random, low-level, spurious interference signals.

B.7 Phase Measurement and Channel Synchronization

See Motherboard, Sheet 2 of 4.

The ability to align the phase of the clock outputs between all clock channels is an important feature of the CG792s. For high-frequency clocks the phase can be adjusted by running slightly off-frequency for a known period of time. For low frequency clocks, the phase can also be adjusted by altering (re-starting, lengthening, or shortening) the FPGA clock divider.

For example, suppose Clocks 1&2 are both running at 1kHz, and the user requests that they be phase aligned. The LMX2572 clocks on both output channels will be running at 20MHz, and their FPGAs will be set to divide by 20,000. To align the phases of the two clock channels, the analog phase detector will first align their LMX2572 clocks to 90 degrees (where the output of the phase detector is zero), then dead-reckon them back to zero degrees. Next, the MPU will assert an MPU_SYNC_RQ that will be re-sync'd to Clock 1 to create FPGA_SYNC. The FPGA_SYNC signal will be passed to all clock channels, and be re-sync'd to the local LMX2572 clock on each board. Finally, the FPGAs for channel 1&2 will be programmed to restart their dividers on the rising edge of the FPGA_SYNC signal, thereby aligning the phase of clocks 1&2.

To enable these measurements, copies of the LMX2572 RF clock, and the FPGA divided clock, are brought to the motherboard via SATA cables (connecting at P300-P303) from each clock channel. Two RF clocks are selected by high-speed analog multiplexers, U302 and U305. The LVPECL clocks are enabled by their termination (RN300 and R320). Their relative phase is measured by the LVPECL XOR gate, U304. The differential output from the XOR phase detector is low pass filtered to provide a differential dc voltage between ±PHASE_DET_OUT. The +1.65 V common mode voltage on this differential signal allows it to be measured directly by one of the MPU's differential input ADCs.

The high-speed analog multiplexers require their power supplies be shifted above ground and +3.3 V in order to accommodate the LVPECL level signals used in this design. A dual op amp, U300, provides these bias voltages. (Less than 1 mA is needed from MPX_VCC and MPX_GND.) The logic signals which control the multiplexers will also need to be shifted. A triple, SPDT switch is used to covert RF_MPX_SEL, LO_MPX_SEL, and PHASE_EN to the correct levels. One LVPECL differential clock is selected to generate the FPGA_SYNC. The termination (R321-R325), enables only the selected clock; all other clocks remain quiet. The selected clock is converted to single-ended logic by U308, which clocks the LVC flip-flop, U309. The FPGA_SYNC occurs on the first rising edge of the selected clock after the MPU_SYNC_RQ is asserted by the MPU.

B.8 MPU and Interfaces

See Motherboard, Sheet 3 of 4.

The CG792s use a Kinetis MPU (U201), which is a 32-bit, single-core ARM running at 100 MHz, with 128k x 8 RAM and 1M x 8 flash ROM. The device has ADCs and DACs, SPI ports, UARTs, and USB/Ethernet connectivity. After booting, the 50 MHz MPU clock, applied to EXTAL0, is sourced from the LMK05318B.

The MPU supports 10/100 Mbit/s Ethernet via a RMII interface. The Ethernet PHY (U208) connects directly to an RJ-45 connector (U207) which includes the magnetics required for the LAN. The 25 MHz clock for the Ethernet PHY is provided by the MPU.

The USB interface is via an FT230Q (U202) UART bridge, for which well-supported MS Windows interface drivers are readily available. The UART/USB bridge is held in reset until the user connects their USB cable to J202. All USB lines are protected against ESD by either U203 or D200. The USB bridge connects to the MPU via UART1.

An RS-232 interface is provided on the rear panel using the MPU's UART0 via a level-shifting line driver, U209. The RS-232 interface can be set to various baud rates and uses RTS/CTS for flow control.

Two other MPU UARTs are used internally. UART2 is used in development as the bootloader for the front panel GPU and UART4 is used to communicate with the (optional) rubidium timebase option.

The MPU has several ADCs, some of which have differential inputs. All of the ADC values are referenced to +3.00VREF2 applied at VREFH. The ADCs are used to measure the clock channel phase detector output (with zero volts indicative of a 90° phase relationship), a selected signal on ±MPX_ANALOG (one of eight analog test points from either vertical PCB), analog test points from the optional OCXO (HEAT_MON, VARAC_MON, AND AGC_MON), the voltage at the Analog Modulation Input (±MOD_IN), the amplitude of the 10 MHz external timebase reference, and the system power supply voltages (+24V, ±10V, ±5V, +3.3V, and +3.00VREF).

Two comparator inputs to the MPU (+3.3V/2 and +24V/9) can be used to generate interrupts in the case that the system power supplies are going down.

There are three SPI ports.

SPI_0 is used to configure the small motherboard FPGA (using CS_MB_FPGA), and to communicate with the vertical PCBs (using CS_SR_FRONT and CS_SR_REAR) and the clock channel cards (using CS_ETC_FRONT

and CS_ETC_REAR). This SPI port will be active during start-up and whenever a clock channel setting is changed, otherwise it will be quiet.

SPI_1 is used for communications with the front panel GPU and GUI. As this communications path might have a lot of traffic, LVDS signaling is used for both the SPI clock and data.

SPI_2 is used to configure the LMK05318B (reference frequency generator), and to set the digital potentiometer, U107, (which is used to trim the optional OCXO and rubidium frequency standards). This is referred to as the "Quiet SPI", as it is almost always inactive so as not to disturb the devices which it controls with unintended crosstalk.

There are several GPIO pins on the MPU that are used as single-bit inputs and outputs for various purposes. Primary among these is the power-down soft key. When the front panel Power button is pressed, the open-drain MPU_PD_RQ will go high (using an internal pull-up), for which the MPU will begin a power-down sequence. After the MPU gets confirmation from the user on the front panel GUI, the MPU will assert MPU_CLK_OFF, which will disable the power supply inverter, removing all system power supplies (except for the +24V, which remains on whenever the instrument is connected to the mains).

The functionality of other I/O bits is described in the table below.

Name	I/O	Pullup	Description
-RB_INSTALLED	In	Yes	Open drain pulled low if optional rubidium standard is installed
-ASSIGN	In	Yes	Two-pin header with functionality TBD
-ENET_LED	Out		Pulled low to indicate Ethernet traffic
25MHZ_CLKOUT	Out		25 MHz clock output for Ethernet PHY
-RESET In			Pulled low by POR (U200) or PCB button (S200)
PS_SYNC	Out		200 kHz clock to sync inverter in power supply module
REFSEL Out			To LMK05318 to select between Ext or Opt timebases
-EXT_10MHZ_EN	Out		Enable comparator for Ext timebase (after signal detected)
-OPT_10MHZ_EN	Out		Enable comparator for Opt timebase (if installed and no Ext TB)
-RESET_MB_FPGA	Out		Force a reset of the motherboard FPGA
RF_MPX_SEL	Out		Select between Clock 1 and Clock 4 as "RF" mixer input
LO_MPX_SEL	Out		Select between Clock 2 and Clock 3 as "LO" mixer input
-PHASE_EN	Out		Enable phase detector's input multiplexers
-SYNC_EN	Out		Enable FPGA_SYNCs (for alignment of clocks < 12.5 MHz)
SYNC_SEL0	Out		Select clock for FPGA_SYNC master (lowest frequency clock)
SYNC_SEL1	Out		Select clock for FPGA_SYNC master (lowest frequency clock)
MPU_SYNC_RQ	Out		MPU initiates the FPGA_SYNC and waits for FPGA_SYNC_MB
FPGA_SYNC_MB	In		Asserted when the requested FPGA_SYNC has occurred
-EN_DIG_MOD	Out		Enable comparator for external Digital Modulation Input
-BEEP Out			Enables a piezo beeper (100 dBA at about 3.5 kHz)

The front panel GUI connects to the motherboard via a 30-pin jumper cable connecting at J203. In addition to the LVDS SPI lines (and their chip selects) the connector provides +24V, +5V and +3.3V power, and an LVDS reference clock (sourced by the motherboard FPGA at either 1 MHz or 25 MHz, TBD). The front panel "soft" power button, and "Standby LED" are also directly connected to the motherboard.

The MPU has a JTAG port, supporting both the NPX EzPort and J-Link formats, for use during the product's development.

B.9 Power and Voltage References

See Motherboard, Sheet 4 of 4.

A separate, fully enclosed, power supply module holds an always-on, off-line, +24 V SMPS. The +24 V supply can also power another SMPS in the power module, which can be turned on and off. The outputs from the second, bipolar SMPS, are further conditioned by linear regulators to provide very quiet ±10 V, ±5 V, and +3.3 V, all of which are available on the power supply interface connector, J400.

The front panel soft key power switch provides a momentary contact to ground. The bipolar SMPS can be turned off by -DISABLE which is set on power-up, or by a 4 second press of the power button, or by a rising edge of the MPU_CLK_OFF line from the MPU (as requested by MPU_PD_RQ and okayed by the user via the front panel GUI). The bipolar SMPS inverter is enabled when -DISABLE goes low which is done by a short press of the front panel power button.

Two LDO linear regulators, U400 and U402, provide the +2.5 V and +1.2 V supplies required by the small FPGAs used in the instrument.

A +5.00 V reference, U405, provides several voltage references for the system. The +5.00VREF is attenuated, and buffered (by U406) to provide two isolated +3.00 V references.

B.10 Front Panel Interface

See CG792 Front panel, Sheet 1 of 2.

This PCB connects to the motherboard via a 30-pin ribbon cable at J100. The motherboard provides power and an SPI interface via LVDS data lines. There are three SPI devices. GPU_CS1 is used to load two series 8-bit shift registers, and to enable GPU_MISO data from the GPU. The first shift register controls the reset and boot mode of the GPU and the second controls the eight front panel LEDs. (The front panel POWER LED is on whenever the +3.3V power is on, and the STANDBY LED is powered by a signal from the motherboard.) The GPU_CS1 and GPU_CS2 are ports inside of the GPU (on Sheet 2 of 2).

B.11 Front Panel GUI

See CG792 Front panel, Sheet 2 of 2.

The TFT, LCD, IPS display is a ATM0500D27B-CT is 5" (diagonal), with 800x 480 (RGB) resolution, connecting to the PCB at J203. The capacitive touch screen uses a different connector, J205. The LCD's LED backlighting power is sourced from +24V, with the LED current being passed through Q200 and controlled by the GPU's PWM output duty cycle.

The GPU (U201) is an NXP i.MXRT1052, running at 600 MHz, with 512k x 8 RAM on a 196-pin BGA. The GPU clock reference can be either the 24 MHz crystal (as required to support USB operation and the nominal GPU reference frequency) or some other clock frequency (typically 25 MHz, provided directly by ±GPU_CLK_REF from the motherboard). The 24 MHz crystal oscillator can also be phase locked using U204 as a phase detector (comparing the phase between a 1 MHz ±GPU_CLK_REF and the 1 MHz PWM from the GPU) to control the varactor, U206, to lock the crystal oscillator locking its frequency to 24 MHz.

Three front panel push buttons (Clock On/Off, and Increment Up/-Down) are read by the GPU at three GPIO pins with resistive pull-ups. The GPU will then message the MPU on the motherboard when the buttons are pressed.

A fast 16M x 16 SDRAM is connected to the GPU via a 16-bit, bidirectional, parallel data bus. This memory provides the frame buffer for the LCD display, and so there is a lot of data traffic, moving all the time.

A 64 Mb serial flash, with a four-bit data bus, is fast enough (133 MHz) to allow the GPU to execute code from it. There is a vertical mount micro-USB connector, J204, to allow serial boot load of GPU from a computer. Access from rear of front panel PCB. (For development only.)

B.12 Off-Line Power Supply

See Power module, Sheet 1 of 1.

For safety, shielding, and modular assembly, the CG792 uses an enclosed power supply, with a line-cord input and 10-pin × 0.156" female connector output, that provides multiple low-noise, linearly regulated power supplies to the motherboard.

The power supply uses an OEM off-line SMPS that provides +24 Vdc whenever it is connected to the mains. This power supply is not switched off, and so keeps the optional timebase (either an OCXO or a rubidium frequency standard) operating continuously while the instrument is in "Standby".

The off-line switcher is followed by another SMPS which is enabled when the unit is turned on. This SMPS is operated near 100 % duty cycle, with the transformer (T1) primaries being driven by MOSFETs (Q3 and Q4) which are driven by an LM5030 SMPS controller, U7.

The SMPS controller can drive gate currents in excess of 1 A, turning the MOSFET gates on via low value gate resistors (R19 and R20), and turning them off more quickly via the diodes, D18 and D19. The SMPS controller has a soft-start (C27) and can provides over-current protection, sensing the primary side current in the low-value shunt resistor (R23).

The transformer secondaries are full-wave rectified to provide voltages for the linear regulators which follow. RC snubbers (R2/C2 for example) catch the ring from the transformer's leakage inductance. LC low-pass filters L1/C5/C6 for example) greatly attenuate the ripple in the rectified voltage waveform. Low dropout regulators (U5, U6 and U8) provide outputs at ±5 V and +3.3 V. Adjustable regulators (U2 and U4) provide either ±15 V (when P1 is populated) or ±10 V (when P2 is populated).

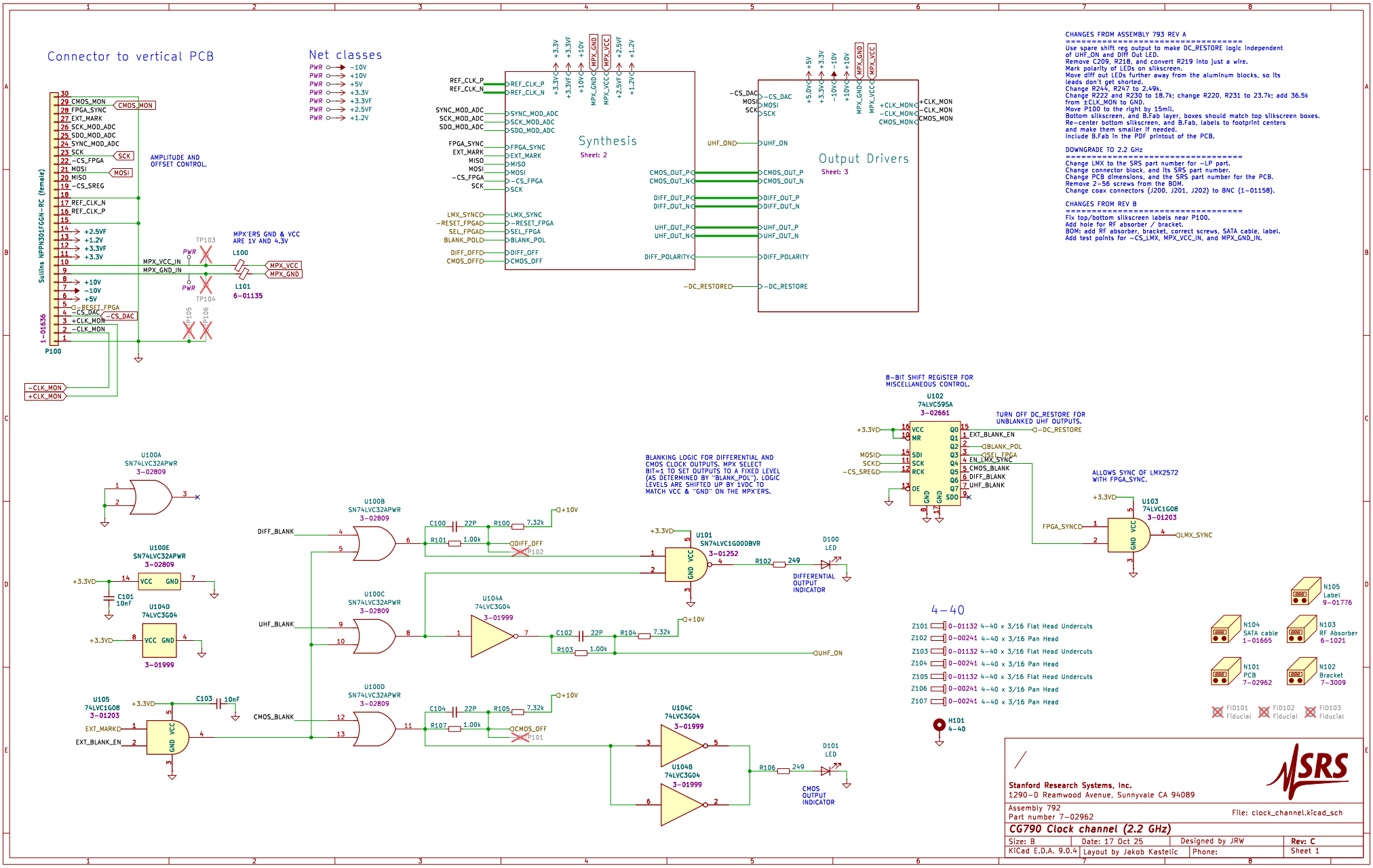
Schottky diodes at each output prevent the outputs from becoming reverse biased during start-up.

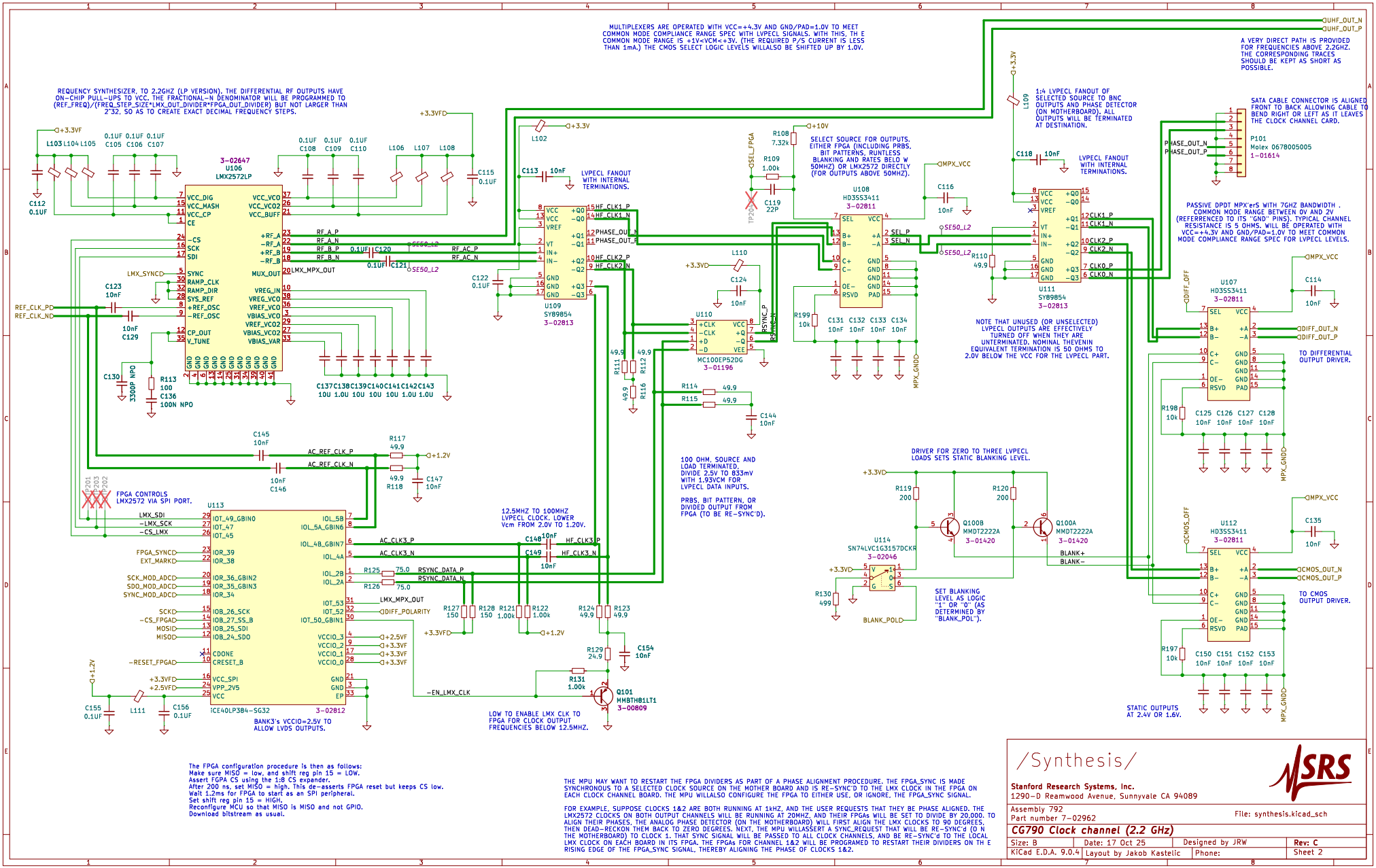
A thermostatically controlled fan, connected at J3, turns on when the power supply is enabled. The voltage applied to the fan, and so the speed of the fan, will increase with the temperature sensed by a 100 kΩ NTC thermistor (R8) on the PCB. The fan voltage will be about 9.5 V for PCB temperatures below 25 °C and increase monotonically to above 20 V at 40 °C. Doing so reduces the fan noise, and reduces all circuit tempcos in the instrument.

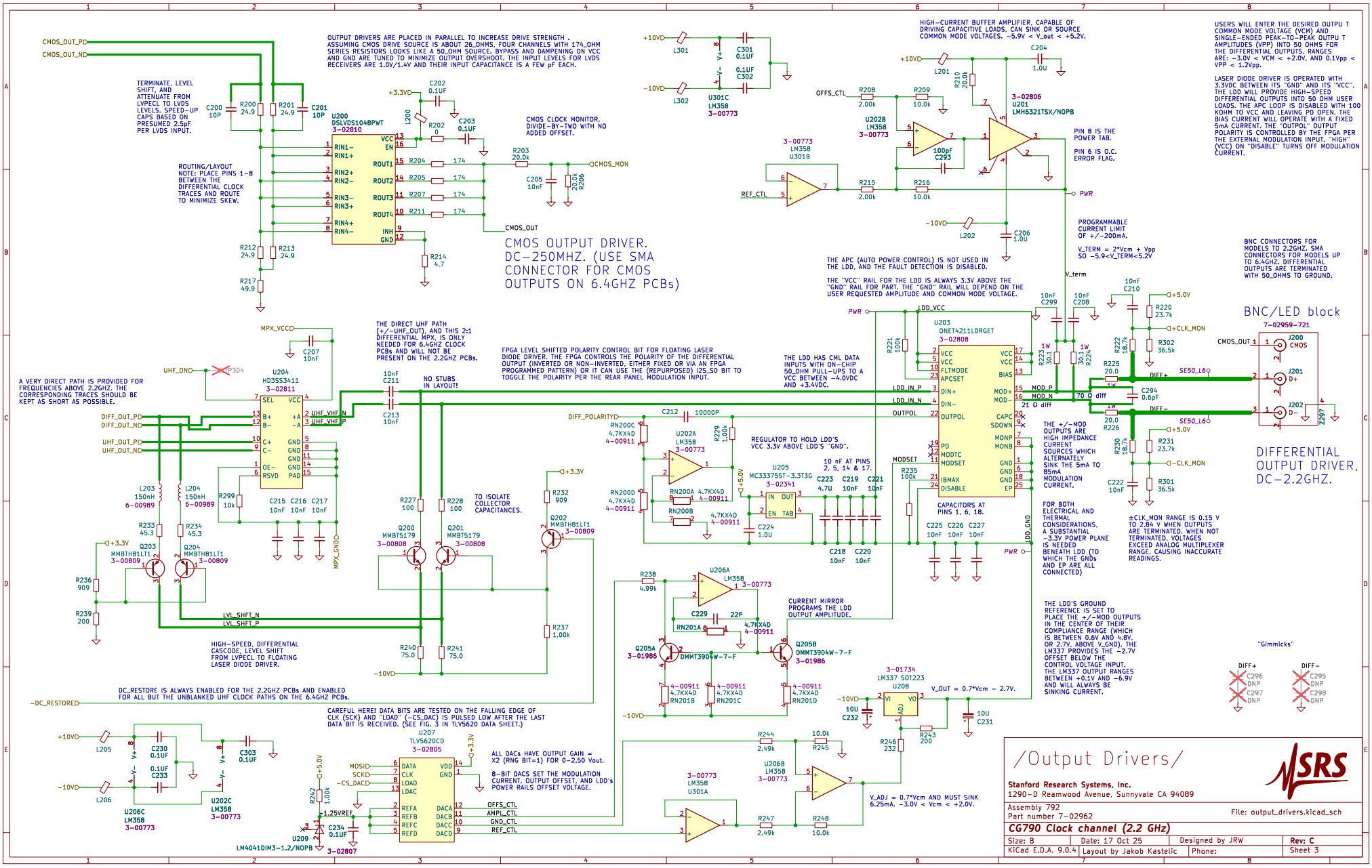
Appendix C Schematic Diagrams

The circuit schematics include:

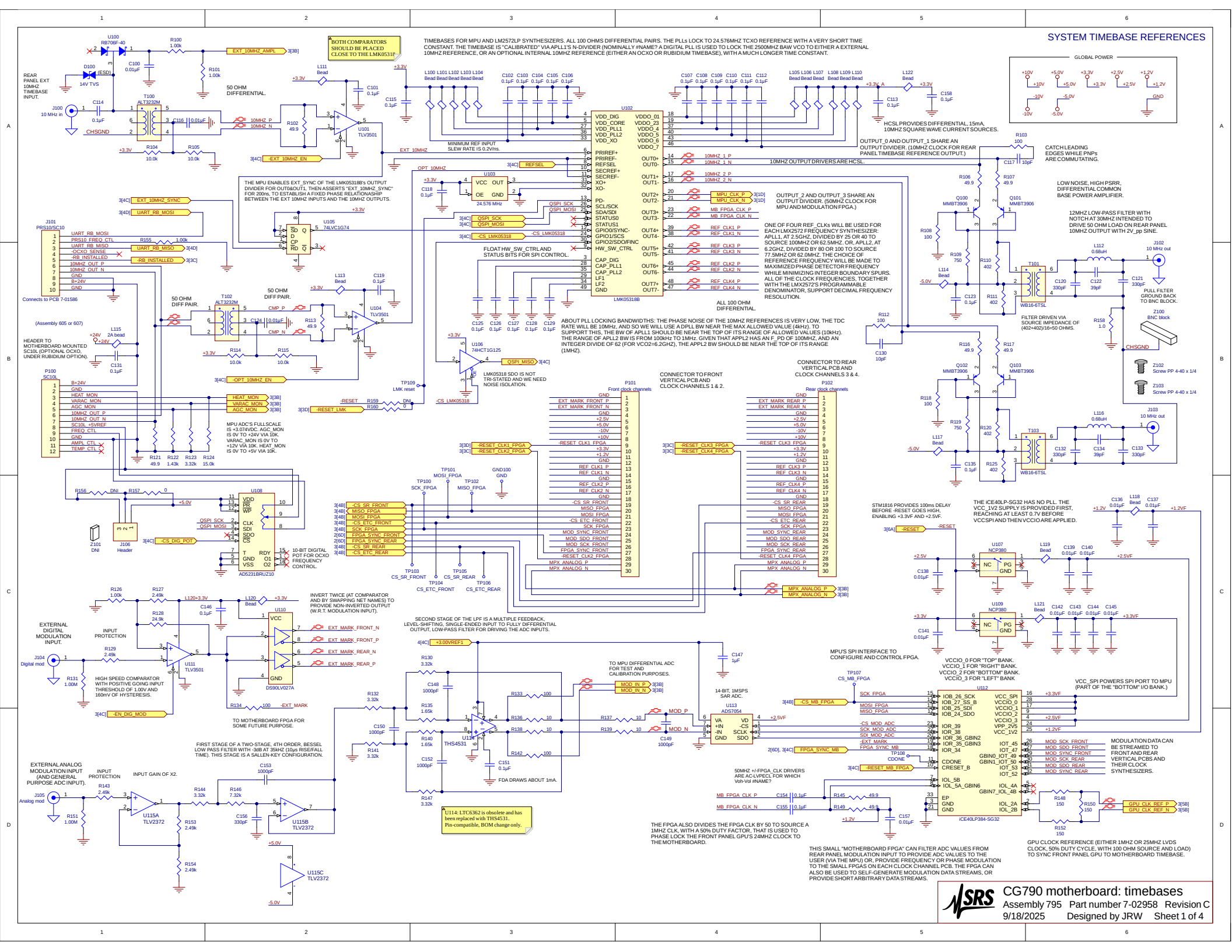
1. **Clock channel cards** with an RF synthesizer operating from 12.5 MHz to 2.2 GHz and a small FPGA for divided outputs below 12.5 MHz (and to provide modulation control of the RF synthesizer), a single-ended CMOS output driver providing a +3.3V square wave via 50 Ω, and high-speed differential outputs able to drive 50 Ω loads to all common high-speed logic levels with 40p◎s transition times. (On three schematic pages.)
2. **Small vertical PCBs** for connecting either front or rear clock channel cards to the mother board. (On one schematic page.)
3. **The Motherboard,** with a system timing references, interfaces to clock channel cards, analog and digital input modulation processing, precision inter-channel phase measurement and synchronization circuitry, an MPU with Ethernet, USB, and RS-232, interfaces reference voltages, and power supply interfaces. (On four schematic pages.)
4. **The graphical user interface** with a high-resolution, color, IPS TFT LCD display with a capacitive touch screen interface. (On two schematic pages.)
5. **A self-enclosed power supply** to provide a variety of low noise power supplies for the instrument, operating from an OEM, off-line, SMPS, and with a thermostatically controlled ventilation fan. (On one schematic page.)
6. **Vertical boards** to connect output channels to the motherboard.


Connector to vertical PCB
Sullins NPPN301FFGN-RC (female)
1-01636
P100
CMOS_MON
FPGA_SYNC
EXT_MARK
SCK_MOD_ADC
SDO_MOD_ADC
SYNC_MOD_ADC
SCK
-CS_FPGA
MOSI
MISO
-CS_SREG
REF_CLK_N
REF_CLK_P
+2.5VF
+1.2V
+3.3VF
+3.3V
+10V
-10V
+5V
-RESET_FPGA
-CS_DAC
+CLK_MON
-CLK_MON
AMPLITUDE AND OFFSET CONTROL.
MPX'ERS GND & VCC ARE 1V AND 4.3V
L100
L101
6-01135
TP103
TP104
TP105
TP106
MPX_VCC_IN
MPX_GND_IN
MPX_VCC
MPX_GND
Net classes
Synthesis
Sheet: 2
Output Drivers
Sheet: 3
CHANGES FROM ASSEMBLY 793 REV A
Use spare shift reg output to make DC_RESTORE logic independent of UHF_ON and Diff Out LED.
Remove C209, R218, and convert R219 into just a wire.
Mark polarity of LEDs on silkscreen.
Move diff out LEDs further away from the aluminum blocks, so its leads don't get shorted.
Change R244, R247 to 2.49k.
Change R222 and R230 to 18.7k; change R220, R231 to 23.7k; add 36.5k from ±CLK_MON to GND.
Move P100 to the right by 15mil.
Bottom silkscreen, and B.Fab layer, boxes should match top silkscreen boxes.
Re-center bottom silkscreen, and B.Fab, labels to footprint centers and make them smaller if needed.
Include B.Fab in the PDF printout of the PCB.
DOWNGRADE TO 2.2 GHz
Change LMX to the SRS part number for -LP part.
Change connector block, and its SRS part number.
Change PCB dimensions, and the SRS part number for the PCB.
Remove 2-56 screws from the BOM.
Change coax connectors (J200, J201, J202) to BNC (1-01158).
CHANGES FROM REV B
Fix top/bottom silkscreen labels near P100.
Add hole for RF absorber / bracket.
BOM: add RF absorber, bracket, correct screws, SATA cable, label.
Add test points for -CS_LMX, MPX_VCC_IN, and MPX_GND_IN.
8-BIT SHIFT REGISTER FOR MISCELLANEOUS CONTROL.
U102
74LVC595A
3-02661
TURN OFF DC_RESTORE FOR UNBLANKED UHF OUTPUTS.
EXT_BLANK_EN
BLANK_POL
SEL_FPGA
EN_LMX_SYNC
CMOS_BLANK
DIFF_BLANK
UHF_BLANK
ALLOWS SYNC OF LMX2572 WITH FPGA_SYNC.
U103
74LVC1G08
3-01203
LMX_SYNC
BLANKING LOGIC FOR DIFFERENTIAL AND CMOS CLOCK OUTPUTS. MPX SELECT BIT=1 TO SET OUTPUTS TO A FIXED LEVEL (AS DETERMINED BY "BLANK_POL"). LOGIC LEVELS ARE SHIFTED UP BY 1VDC TO MATCH VCC & "GND" ON THE MPX'ERS.
U100A
SN74LVC32APWR
3-02809
U100B
U100C
U100D
U100E
U101
SN74LVC1G00DBVR
3-01252
U104A
74LVC3G04
3-01999
U104B
U104C
U104D
U105
74LVC1G08
3-01203
C100 22P
C101 10nF
C102 22P
C103 10nF
C104 22P
C105 22P
R100 7.32k
R101 1.00k
R102 249
R103 1.00k
R104 7.32k
R105 7.32k
R106 249
DIFF_OFF
CMOS_OFF
UHF_ON
D100
LED
DIFFERENTIAL OUTPUT INDICATOR
D101
CMOS OUTPUT INDICATOR
4-40
Z101 0-01132 4-40 x 3/16 Flat Head Undercuts
Z102 0-00241 4-40 x 3/16 Pan Head
Z103 0-01132 4-40 x 3/16 Flat Head Undercuts
Z104 0-00241 4-40 x 3/16 Pan Head
Z105 0-01132 4-40 x 3/16 Flat Head Undercuts
Z106 0-00241 4-40 x 3/16 Pan Head
Z107 0-00241 4-40 x 3/16 Pan Head
H101 4-40
N105 Label 9-01776
N104 SATA cable 1-01665
N103 RF Absorber 6-1021
N101 PCB 7-02962
N102 Bracket 7-3009
FID101 Fiducial
FID102 Fiducial
FID103 Fiducial
Stanford Research Systems, Inc.
1290-D Reamwood Avenue, Sunnyvale CA 94089
Assembly 792
Part number 7-02962
File: clock_channel.kicad_sch
CG790 Clock channel (2.2 GHz)
Size: B
Date: 17 Oct 25
Designed by JRW
Rev: C
KiCad E.D.A. 9.0.4
Layout by Jakob Kastelic
Phone:
Sheet 1


MULTIPLEXERS ARE OPERATED WITH VCC=+4.3V AND GND/PAD=1.0V TO MEET COMMON MODE COMPLIANCE RANGE SPEC WITH LVPECL SIGNALS. WITH THIS, TH E COMMON MODE RANGE IS +1V<VCM<+3V. (THE REQUIRED P/S CURRENT IS LESS THAN 1mA.) THE CMOS SELECT LOGIC LEVELS WILLALSO BE SHIFTED UP BY 1.0V.
REQUENCY SYNTHESIZER, TO 2.2GHZ (LP VERSION). THE DIFFERENTIAL RF OUTPUTS HAVE ON-CHIP PULL-UPS TO VCC. THE FRACTIONAL-N DENOMINATOR WILL BE PROGRAMMED TO (REF_FREQ)/(FREQ_STEP_SIZE*LMX_OUT_DIVIDER*FPGA_OUT_DIVIDER) BUT NOT LARGER THAN 2^32, SO AS TO CREATE EXACT DECIMAL FREQUENCY STEPS.
3-02647
U106
LMX2572LP
SELECT SOURCE FOR OUTPUTS. EITHER FPGA (INCLUDING PRBS, BIT PATTERNS, RUNTLESS BLANKING AND RATES BELO W 50MHZ) OR LMX2572 DIRECTLY (FOR OUTPUTS ABOVE 50MHZ).
LVPECL FANOUT WITH INTERNAL TERMINATIONS.
U108
HD3SS3411
3-02811
U109
SY89854
3-02813
U110
MC100EP52DG
3-01196
1:4 LVPECL FANOUT OF SELECTED SOURCE TO BNC OUTPUTS AND PHASE DETECTOR (ON MOTHERBOARD). ALL OUTPUTS WILL BE TERMINATED AT DESTINATION.
A VERY DIRECT PATH IS PROVIDED FOR FREQUENCIES ABOVE 2.2GHZ. THE CORRESPONDING TRACES SHOULD BE KEPT AS SHORT AS POSSIBLE.
SATA CABLE CONNECTOR IS ALIGNED FRONT TO BACK ALLOWING CABLE TO BEND RIGHT OR LEFT AS IT LEAVES THE CLOCK CHANNEL CARD.
P101
Molex 0678005005
1-01614
PASSIVE DPDT MPX'erS WITH 7GHZ BANDWIDTH . COMMON MODE RANGE BETWEEN 0V AND 2V (REFERRENCED TO ITS "GND" PINS). TYPICAL CHANNEL RESISTANCE IS 5 OHMS. WILL BE OPERATED WITH VCC=+4.3V AND GND/PAD=1.0V TO MEET COMMON MODE COMPLIANCE RANGE SPEC FOR LVPECL LEVELS.
NOTE THAT UNUSED (OR UNSELECTED) LVPECL OUTPUTS ARE EFFECTIVELY TURNED OFF WHEN THEY ARE UNTERMINATED. NOMINAL THEVENIN EQUIVALENT TERMINATION IS 50 OHMS TO 2.0V BELOW THE VCC FOR THE LVPECL PART.
U111
SY89854
3-02813
U107
HD3SS3411
3-02811
TO DIFFERENTIAL OUTPUT DRIVER.
U112
HD3SS3411
3-02811
TO CMOS OUTPUT DRIVER.
STATIC OUTPUTS AT 2.4V OR 1.6V.
100 OHM, SOURCE AND LOAD TERMINATED. DIVIDE 2.5V TO 833mV WITH 1.93VCM FOR LVPECL DATA INPUTS.
PRBS, BIT PATTERN, OR DIVIDED OUTPUT FROM FPGA (TO BE RE-SYNC'D).
12.5MHZ TO 100MHZ LVPECL CLOCK. LOWER Vcm FROM 2.0V TO 1.20V.
DRIVER FOR ZERO TO THREE LVPECL LOADS SETS STATIC BLANKING LEVEL.
Q100B
MMDT2222A
3-01420
Q100A
MMDT2222A
3-01420
U114
SN74LVC1G3157DCKR
3-02046
SET BLANKING LEVEL AS LOGIC "1" OR "0" (AS DETERMINED BY "BLANK_POL").
FPGA CONTROLS LMX2572 VIA SPI PORT.
U113
iCE40LP384-SG32
3-02812
BANK3's VCCIO=2.5V TO ALLOW LVDS OUTPUTS.
LOW TO ENABLE LMX CLK TO FPGA FOR CLOCK OUTPUT FREQUENCIES BELOW 12.5MHZ.
Q101
MMBTH81LT1
3-00809
The FPGA configuration procedure is then as follows:
Make sure MISO = low, and shift reg pin 15 = LOW.
Assert FGPA CS using the 1:8 CS expander.
After 200 ns, set MISO = high. This de-asserts FPGA reset but keeps CS low.
Wait 1.2ms for FPGA to start as an SPI peripheral.
Set shift reg pin 15 = HIGH.
Reconfigure MCU so that MISO is MISO and not GPIO.
Download bitstream as usual.
THE MPU MAY WANT TO RESTART THE FPGA DIVIDERS AS PART OF A PHASE ALIGNMENT PROCEDURE. THE FPGA_SYNC IS MADE SYNCHRONOUS TO A SELECTED CLOCK SOURCE ON THE MOTHER BOARD AND IS RE-SYNC'D TO THE LMX CLOCK IN THE FPGA ON EACH CLOCK CHANNEL BOARD. THE MPU WILLALSO CONFIGURE THE FPGA TO EITHER USE, OR IGNORE, THE FPGA_SYNC SIGNAL.
FOR EXAMPLE, SUPPOSE CLOCKS 1&2 ARE BOTH RUNNING AT 1kHZ, AND THE USER REQUESTS THAT THEY BE PHASE ALIGNED. THE LMX2572 CLOCKS ON BOTH OUTPUT CHANNELS WILL BE RUNNING AT 20MHZ, AND THEIR FPGAs WILL BE SET TO DIVIDE BY 20,000. TO ALIGN THEIR PHASES, THE ANALOG PHASE DETECTOR (ON THE MOTHERBOARD) WILL FIRST ALIGN THE LMX CLOCKS TO 90 DEGREES, THEN DEAD-RECKON THEM BACK TO ZERO DEGREES. NEXT, THE MPU WILLASSERT A SYNC_REQUEST THAT WILL BE RE-SYNC'd (O N THE MOTHERBOARD) TO CLOCK 1. THAT SYNC SIGNAL WILL BE PASSED TO ALL CLOCK CHANNELS, AND BE RE-SYNC'd TO THE LOCAL LMX CLOCK ON EACH BOARD IN ITS FPGA. THE FPGAs FOR CHANNEL 1&2 WILL BE PROGRAMED TO RESTART THEIR DIVIDERS ON TH E RISING EDGE OF THE FPGA_SYNC SIGNAL, THEREBY ALIGNING THE PHASE OF CLOCKS 1&2.
/Synthesis/
Stanford Research Systems, Inc.
1290-D Reamwood Avenue, Sunnyvale CA 94089
Assembly 792
Part number 7-02962
File: synthesis.kicad_sch
CG790 Clock channel (2.2 GHz)
Size: B
Date: 17 Oct 25
Designed by JRW
Rev: C
KiCad E.D.A. 9.0.4
Layout by Jakob Kastelic
Phone:
Sheet 2


CMOS OUTPUT DRIVER.
DC-250MHZ. (USE SMA CONNECTOR FOR CMOS OUTPUTS ON 6.4GHZ PCBs)
OUTPUT DRIVERS ARE PLACED IN PARALLEL TO INCREASE DRIVE STRENGTH . ASSUMING CMOS DRIVE SOURCE IS ABOUT 26_OHMS, FOUR CHANNELS WITH 174_OHM SERIES RESISTORS LOOKS LIKE A 50_OHM SOURCE. BYPASS AND DAMPENING ON VCC AND GND ARE TUNED TO MINIMIZE OUTPUT OVERSHOOT. THE INPUT LEVELS FOR LVDS RECEIVERS ARE 1.0V/1.4V AND THEIR INPUT CAPACITANCE IS A FEW pF EACH.
TERMINATE, LEVEL SHIFT, AND ATTENUATE FROM LVPECL TO LVDS LEVELS, SPEED-UP CAPS BASED ON PRESUMED 2.5pF PER LVDS INPUT.
ROUTING/LAYOUT NOTE: PLACE PINS 1-8 BETWEEN THE DIFFERENTIAL CLOCK TRACES AND ROUTE TO MINIMIZE SKEW.
CMOS CLOCK MONITOR. DIVIDE-BY-TWO WITH NO ADDED OFFSET.
HIGH-CURRENT BUFFER AMPLIFIER, CAPABLE OF DRIVING CAPACITIVE LOADS, CAN SINK OR SOURCE COMMON MODE VOLTAGES. -5.9V < V_out < +5.2V.
PIN 8 IS THE POWER TAB.
PIN 6 IS O.C. ERROR FLAG.
USERS WILL ENTER THE DESIRED OUTPU T COMMON MODE VOLTAGE (VCM) AND SINGLE-ENDED PEAK-TO-PEAK OUTPU T AMPLITUDES (VPP) INTO 50 OHMS FOR THE DIFFERENTIAL OUTPUTS. RANGES ARE: -3.0V < VCM < +2.0V, AND 0.1Vpp < VPP < 1.2Vpp.
LASER DIODE DRIVER IS OPERATED WITH 3.3VDC BETWEEN ITS "GND" AND ITS "VCC". THE LDD WILL PROVIDE HIGH-SPEED DIFFERENTIAL OUTPUTS INTO 50 OHM USER LOADS. THE APC LOOP IS DISABLED WITH 100 KOHM TO VCC AND LEAVING PD OPEN. THE BIAS CURRENT WILL OPERATE WITH A FIXED 5mA CURRENT. THE "OUTPOL" OUTPUT POLARITY IS CONTROLLED BY THE FPGA PER THE EXTERNAL MODULATION INPUT. "HIGH" (VCC) ON "DISABLE" TURNS OFF MODULATION CURRENT.
PROGRAMMABLE CURRENT LIMIT OF +/-200mA.
V_TERM = 2*Vcm + Vpp
SO -5.9<V_TERM<5.2V
THE APC (AUTO POWER CONTROL) IS NOT USED IN THE LDD, AND THE FAULT DETECTION IS DISABLED.
THE "VCC" RAIL FOR THE LDD IS ALWAYS 3.3V ABOVE THE "GND" RAIL FOR PART. THE "GND" RAIL WILL DEPEND ON THE USER REQUESTED AMPLITUDE AND COMMON MODE VOLTAGE.
BNC CONNECTORS FOR MODELS TO 2.2GHZ. SMA CONNECTORS FOR MODELS UP TO 6.4GHZ. DIFFERENTIAL OUTPUTS ARE TERMINATED WITH 50_OHMS TO GROUND.
BNC/LED block
7-02959-721
DIFFERENTIAL OUTPUT DRIVER, DC-2.2GHZ.
THE DIRECT UHF PATH (+/-UHF_OUT), AND THIS 2:1 DIFFERENTIAL MPX, IS ONLY NEEDED FOR 6.4GHZ CLOCK PCBs AND WILL NOT BE PRESENT ON THE 2.2GHZ PCBs.
A VERY DIRECT PATH IS PROVIDED FOR FREQUENCIES ABOVE 2.2GHZ. THE CORRESPONDING TRACES SHOULD BE KEPT AS SHORT AS POSSIBLE.
NO STUBS IN LAYOUT!
FPGA LEVEL SHIFTED POLARITY CONTROL BIT FOR FLOATING LASER DIODE DRIVER. THE FPGA CONTROLS THE POLARITY OF THE DIFFERENTIAL OUTPUT (INVERTED OR NON-INVERTED, EITHER FIXED OR VIA AN FPGA PROGRAMMED PATTERN) OR IT CAN USE THE (REPURPOSED) I2S_SD BIT TO TOGGLE THE POLARITY PER THE REAR PANEL MODULATION INPUT.
THE LDD HAS CML DATA INPUTS WITH ON-CHIP 50_OHM PULL-UPS TO A VCC BETWEEN -4.0VDC AND +3.4VDC.
REGULATOR TO HOLD LDD'S VCC 3.3V ABOVE LDD'S "GND".
10 nF AT PINS 2, 5, 14 & 17.
CAPACITORS AT PINS 1, 6, 18.
THE +/-MOD OUTPUTS ARE HIGH IMPEDANCE CURRENT SOURCES WHICH ALTERNATELY SINK THE 5mA TO 85mA MODULATION CURRENT.
FOR BOTH ELECTRICAL AND THERMAL CONSIDERATIONS, A SUBSTANTIAL -3.3V POWER PLANE IS NEEDED BENEATH LDD (TO WHICH THE GNDs AND EP ARE ALL CONNECTED)
±CLK_MON RANGE IS 0.15 V TO 2.84 V WHEN OUTPUTS ARE TERMINATED. WHEN NOT TERMINATED, VOLTAGES EXCEED ANALOG MULTIPLEXER RANGE, CAUSING INACCURATE READINGS.
THE LDD'S GROUND REFERENCE IS SET TO PLACE THE +/-MOD OUTPUTS IN THE CENTER OF THEIR COMPLIANCE RANGE (WHICH IS BETWEEN 0.6V AND 4.8V, OR 2.7V, ABOVE V_GND). THE LM337 PROVIDES THE -2.7V OFFSET BELOW THE CONTROL VOLTAGE INPUT. THE LM337 OUTPUT RANGES BETWEEN +0.1V AND -6.9V AND WILL ALWAYS BE SINKING CURRENT.
TO ISOLATE COLLECTOR CAPACITANCES.
CURRENT MIRROR PROGRAMS THE LDD OUTPUT AMPLITUDE.
HIGH-SPEED, DIFFERENTIAL CASCODE, LEVEL SHIFT FROM LVPECL TO FLOATING LASER DIODE DRIVER.
DC_RESTORE IS ALWAYS ENABLED FOR THE 2.2GHZ PCBs AND ENABLED FOR ALL BUT THE UNBLANKED UHF CLOCK PATHS ON THE 6.4GHZ PCBs.
CAREFUL HERE! DATA BITS ARE TESTED ON THE FALLING EDGE OF CLK (SCK) AND "LOAD" (-CS_DAC) IS PULSED LOW AFTER THE LAST DATA BIT IS RECEIVED. (SEE FIG. 3 IN TLV5620 DATA SHEET.)
ALL DACs HAVE OUTPUT GAIN = X2 (RNG BIT=1) FOR 0-2.50 Vout.
8-BIT DACS SET THE MODULATION CURRENT, OUTPUT OFFSET, AND LDD's POWER RAILS OFFSET VOLTAGE.
V_ADJ = 0.7*Vcm AND MUST SINK 6.25mA. -3.0V < Vcm < +2.0V.
V_OUT = 0.7*Vcm - 2.7V.
"Gimmicks"
/Output Drivers/
Stanford Research Systems, Inc.
1290-D Reamwood Avenue, Sunnyvale CA 94089
Assembly 792
Part number 7-02962
File: output_drivers.kicad_sch
CG790 Clock channel (2.2 GHz)
Size: B
Date: 17 Oct 25
Designed by JRW
Rev: C
KiCad E.D.A. 9.0.4
Layout by Jakob Kastelic
Phone:
Sheet 3

SYSTEM TIMEBASE REFERENCES



PHASE DETECTOR AND FPGA SYNC

GLOBAL POWER

+10V -10V +5.0V -5.0V +3.3V +2.5V +1.2V GND

FOUR SATA CABLE CONNECTIONS TO CLOCK SYNTHESIZER PCBs BRING LMX2572 LVPECL "PHASE" AND CHANNEL CLOCK (PERHAPS AFTER FPGA DIVIDE) DOWN TO THE MOTHERBOARD.

P200 SATA connector — CLK1_P, CLK1_N, CLK1_PHASE_P, CLK1_PHASE_N

P201 SATA connector — CLK2_P, CLK2_N, CLK2_PHASE_P, CLK2_PHASE_N

P202 SATA connector — CLK3_P, CLK3_N, CLK3_PHASE_P, CLK3_PHASE_N

P203 SATA connector — CLK4_P, CLK4_N, CLK4_PHASE_P, CLK4_PHASE_N

Matched CLK lengths / Matched phase lengths

LEVEL SHIFT LOGIC FOR THE MULTIPLEXERS.

U201 74HCT4053 — RF_MPX_SEL, LO_MPX_SEL, -PHASE_EN; RF_MPX, LO_MPX, -MPX_EN; MPX_VCC, MPX_GND

PASSIVE DPDT MPXERS WITH 7GHZ BANDWIDTH. COMMON MODE RANGE BETWEEN 0V AND 2V (REFERRENCED TO ITS "GND" PINS). TYPICAL CHANNEL RESISTANCE IS 5 OHMS. WILL BE OPERATED WITH VCC=+4.3V AND GND/PAD=1.0V TO MEET COMMON MODE COMPLIANCE RANGE SPEC FOR LVPECL LEVELS.

U202 HD3SS3411 — CLK1_PHASE_P/N, RF_MPX, CLK4_PHASE_P/N, -MPX_EN; "RF"

U205 HD3SS3411 — CLK2_PHASE_P/N, LO_MPX, CLK3_PHASE_P/N, -MPX_EN; "LO"

R210 4.7k, R221 4.7k

C209 C210 C211 C212 0.01µF — CAPS AT PINS 5, 8, 11 & 14.

C219 C220 C221 C222 0.01µF — CAPS AT PINS 5, 8, 11 & 14.

C204 0.01µF

AN UNSELECTED LVPECL SOURCE IS UNTERMINATED AND SO WILL BE TURNED OFF. ALL WILL BE OFF WHEN -MPX_EN IS HIGH.

LVPECL LOGIC GATE AS AN RF MIXER (DC TO 3.2 GHZ). THE HIGH-BANDWIDTH MULTIPLEXERS ARE USED TO SELECT THE RF AND LO INPUTS FROM AMONG THE FOUR POSSIBLE CLOCK SOURCES.

L200 Bead, C208 0.1µF

U203 100EP08

RN200 47 x 4 LVPECL TERMINATION

C218 0.01µF, R222 24.9

R212 249, R213 249, R214 249, R215 249, R216 49.9, R217 49.9, R220 49.9

C213 470pF, C215 470pF, C216 0.01µF

DIFFERENTIAL GAIN OF 4X, LOW-PASS AMPLIFIER WITH COMMON MODE OUTPUT VOLTAGE OF +3.3V/2=1.65V. THE -3dB POINT IS ABOUT 600kHZ AND THE STOP BAND ATTENUATION AT 25MHZ (THE LOWEST OUTPUT FREQUENCY FROM THE XOR MIXER) IS ABOUT -77dB. WILL BE PASSED TO AN MPU DIFFERENTIAL 12-BIT ADC INPUT TO PROVIDE A RESOLUTION OF 0.045 DEGREE PER BIT (OR MORE WITH MPU'S PGA).

U204 THS4531 — C205 100pF, R209 2.00k, R218 2.00k, C217 100pF, C207 0.1µF, R211 249, R219 249, C214 220pF

Changed from LTC6362 (obsolete)

TO AN MPU DIFFERENTIAL ADC WITH AN INPUT PROGRAMMABLE GAIN AMPLIFIER.

PHASE_DET_OUT_N 3[3B], PHASE_DET_OUT_P 3[3B]

THERE ARE FOUR POSSIBLE PHASE MEASUREMENTS:

RF_MPX	LO_MUX	PHASE MEASUREMENT
0	0	BETWEEN CLOCKS 3&4
0	1	BETWEEN CLOCKS 2&4
1	0	BETWEEN CLOCKS 1&3
1	1	BETWEEN CLOCKS 1&2

ONLY THE SELECTED SYNC CLOCK SOURCE WILL HAVE ITS LVPECL OUTPUTS ENABLED. (DISABLE SYNC WHEN NOT IN USE.) THE SELECTED CLOCK IS TERMINATED, 100 OHM DIFFERENTIAL.

U206 FSUSB74 — CLK1_N/P, CLK2_N/P, CLK3_N/P, CLK4_N/P; MPX_CLK_N, MPX_CLK_P; SEL1, SEL0, -OE, EP, GND

C223 0.1µF

3[4C] -SYNC_EN, SYNC_SEL0, SYNC_SEL1

R223 24.9, R224 24.9, R225 24.9, R226 24.9, R227 49.9

High=2.4V, low=1.3V, P=14 mW

RE-SYNC THE MPU SYNC REQUEST TO ONE OF FOUR CLOCKS. THEN, THAT SYNC SIGNAL, WHICH IS SENT TO EACH CLOCK CHANNEL WILL BE RE-SYNC'D (AS THIS FLIP-FLOP MIGHT BE METASTABLE) TO THE LMX2572 CLOCK, AND MAY THEN BE USED TO RESTART THE CLOCK DIVIDERS IN THE FPGAs.

L201 Bead, U209 SN65LVDS2

3[4C] MPU_SYNC_RQ — U207 74LVC1G74

FPGA_SYNC FANOUT BUFFER. COPIES FOR FRONT CLOCKS, REAR CLOCKS, AND MOTHERBOARD DEVICES (MPU AND FPGA). SYNC IS DONE ON SINGLE RISING EDGE (HENCE NO LVDS DRIVERS).

U208 74LVC3G34 — C224 0.1µF, R228 22, R229 22

FPGA_SYNC_FRONT 1[2C], FPGA_SYNC_REAR 1[2C], FPGA_SYNC_MB 1[4D], 3[4C]

THE SYNC SIGNAL IS USED TO RESTART THE DIVIDERS IN THE FPGAs. CLOCK OUTPUTS ABOVE 25MHZ DO NOT USE FPGA DIVIDERS AND SO DO NOT USE, OR NEED, THE SYNC SIGNAL.

BIAS SOURCES FOR HIGH-BANDWIDTH MULTIPLEXERS. OPERATED WITH VCC=+4.3V AND GND/PAD=1.0V TO MEET COMMON MODE COMPLIANCE RANGE SPEC WITH LVPECL SIGNALS. WITH THIS, THE COMMON MODE RANGE IS +1V<VCM<+3V. THE REQUIRED BIAS CURRENT IS LESS THAN 1mA. THE CMOS SELECT LOGIC LEVELS ARE ALSO SHIFTED TO MPX_VCC & MPX_GND.

U200A U200B U200C LM358 — R200 5.62k, R201 10, R202 3.32k, R203 2.49k, C201 3300pF, R204 1.00k, R205 1.00k, R206 10, R207 2.49k, C203 3300pF, R208 1.00k

MPX_VCC (ABOUT 4.3VDC) — C200 1µF

MPX_GND (ABOUT 1.0VDC) — C202 1µF

STABILIZE OP AMPS FOR CAPACITIVE LOADS.

CG790 motherboard: phase
Assembly 795 Part number 7-02958 Revision C
9/18/2025 Designed by JRW Sheet 2 of 4

JTAG

Cortex Debug+ETM connector
Trace signals must be length matched to within 500 mils

SEGGER wiki says about pins 11 and 13: "This pin can be used to supply power to the target hardware. If you do not plan to supply power to the target via this pin it is recommended to connect it to GND."

Pin 5 is not connected to the motherboard's +5V supply because it is an output from the debugger.

REAR PANEL USB

IN LAYOUT, PLEASE HOME-RUN THE USB AND ETHERNET'S RJ-45 GROUND CONNECTIONS TO A SINGLE POINT GROUND AT A NEARBY PCB TO CHASSIS MOUNTING POINT.

ESD PROTECTION

REPROGRAM FT230 SO THAT -SLEEP OUTPUT BECOMES -KEEP_AWAKE INPUT TO AVOID HANGING PER FDTI ERRATA.

FTDI UART TO USB BRIDGE. THIS PART HAS WHQL DRIVERS THAT ARE QUICKLY DISCOVERED BY MOST WINDOWS COMPUTERS.

USE TO DETECT USER'S USB CONNECTION.

SPI DATA IS USED TO CONFIGURE THE FPGAs ON THE MOTHERBOARD AND ON EACH CLOCK OUTPUT PCB.

HIGH SPEED DATA TRANSFER TO FRONT PANEL GUI AND MEMORY. LVDS DRIVERS AND RECEIVER ARE LOCATED CLOSE TO THE MPU.

DUAL-INLINE CONNECTOR BETWEEN MOTHERBOARD AND THE FRONT PANEL PCB. DIFFERENTIAL PAIRS ARE ADJACENT, AND ARE SEPARATED FROM OTHER DIFFERENTIAL PAIRS BY A GROUND. MOMENTARY SHORTS TO ADJACENT PINS SHOULD CAUSE NO DAMAGE.

GPU CLOCK REFERENCE. EITHER 1MHZ OR 25MHZ AS PROVIDED BY MOTHERBOARD "MODULATION" FPGA.

OPTIONAL OCXO ANALOG

SPI INTERFACE TO FRONT PANEL AND GUI.

SPI VIA LVDS FOR REDUCED EMI ON WHAT MIGHT BE A LOT OF DATA TRAFFIC.

QUIET SPI FOR PRECISION FREQUENCY CONTROL

INTERRUPT ON LOST POWER.

NEED PULL-UPS!

ASSIGNABLE FUNCTIONALITY

MPU_PD_RQ IS OPEN DRAIN (PULL UP PROVIDED BY GPIO INPUT) THAT GOES HIGH WHEN ON/OFF KEY IS PRESSED. MPU WILL CONFIRM POWER DOWN REQUEST ON GUI THEN ASSERT MPU_CLK_OFF TO TURN OFF POWER INVERTER.

THE K64'S USB INTERFACE IS NOT USED BECAUSE THE FDTI UART BRIDGE HAS BETTER WINDOWS DRIVER SUPPORT AND WILL PROVIDE BETTER PROTECTION OF THE MPU FROM ESD.

IDLE AT HIGH LEVEL. PULSE DURATION WILL SET EFFECTIVE LOUDNESS.

DC powered piezo indicator.
Footprint accommodates either:
• 30mm piezo indicator 6-01327-600 or
• 12mm magnetic indicator 6-01339-600
6-01339 is currently specified.

Ethernet

IN LAYOUT, PLEASE HOME-RUN THE USB AND ETHERNET'S RJ-45 GROUND CONNECTIONS TO A SINGLE POINT GROUND AT A NEARBY PCB TO CHASSIS MOUNTING POINT.

(VERY SHORT TRACES!)

ANEN SPEED bootstrap signal is pulled up by LED

ETHERNET FIRMWARE NOTE: THE MPU PORTS USED FOR -ENET_INTRP, -ENET_RESET AND -ENET_LED HAVE BEEN CHANGED FROM THE RGA120.

BE SURE THE 25MHZ CLOCK IS "ON" BEFORE RELEASING -ENET_RESET.

50MHZ CLOCK FROM LMK05318B.

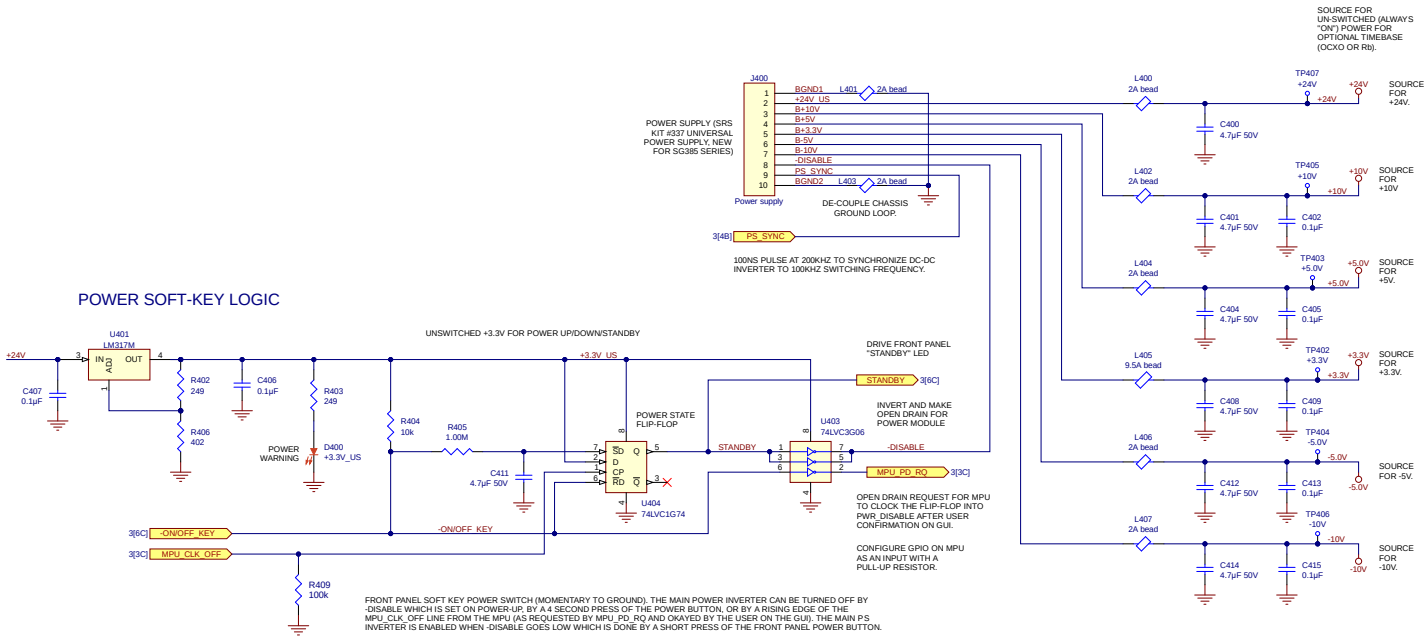
RS-232 TRANSCEIVER

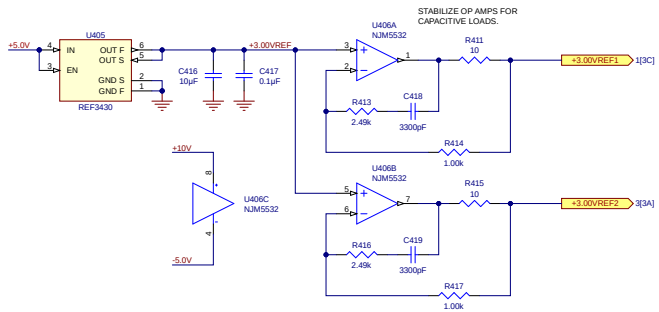
UART2 IS USED FOR THE FRONT PANEL BOOTLOADER AND UART4 IS USED FOR THE RB TIMEBASE.

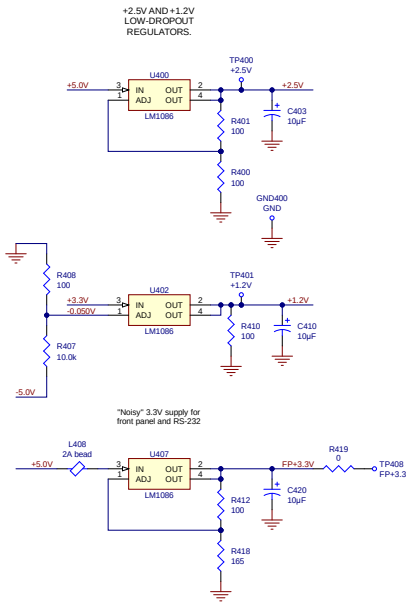
REAR PANEL RS-232 CONNECTOR.

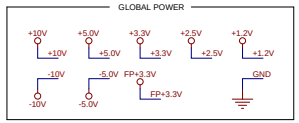
GLOBAL POWER

System power supplies









MOUNTING HOLES: PCB TO CHASSIS

MH400 Mounting hole
MH401 Mounting hole
MH402 Mounting hole
MH403 Mounting hole

F400 Fiducial
F401 Fiducial
F402 Fiducial
F403 Fiducial
F404 Fiducial
F405 Fiducial

ART400 SRS Logo

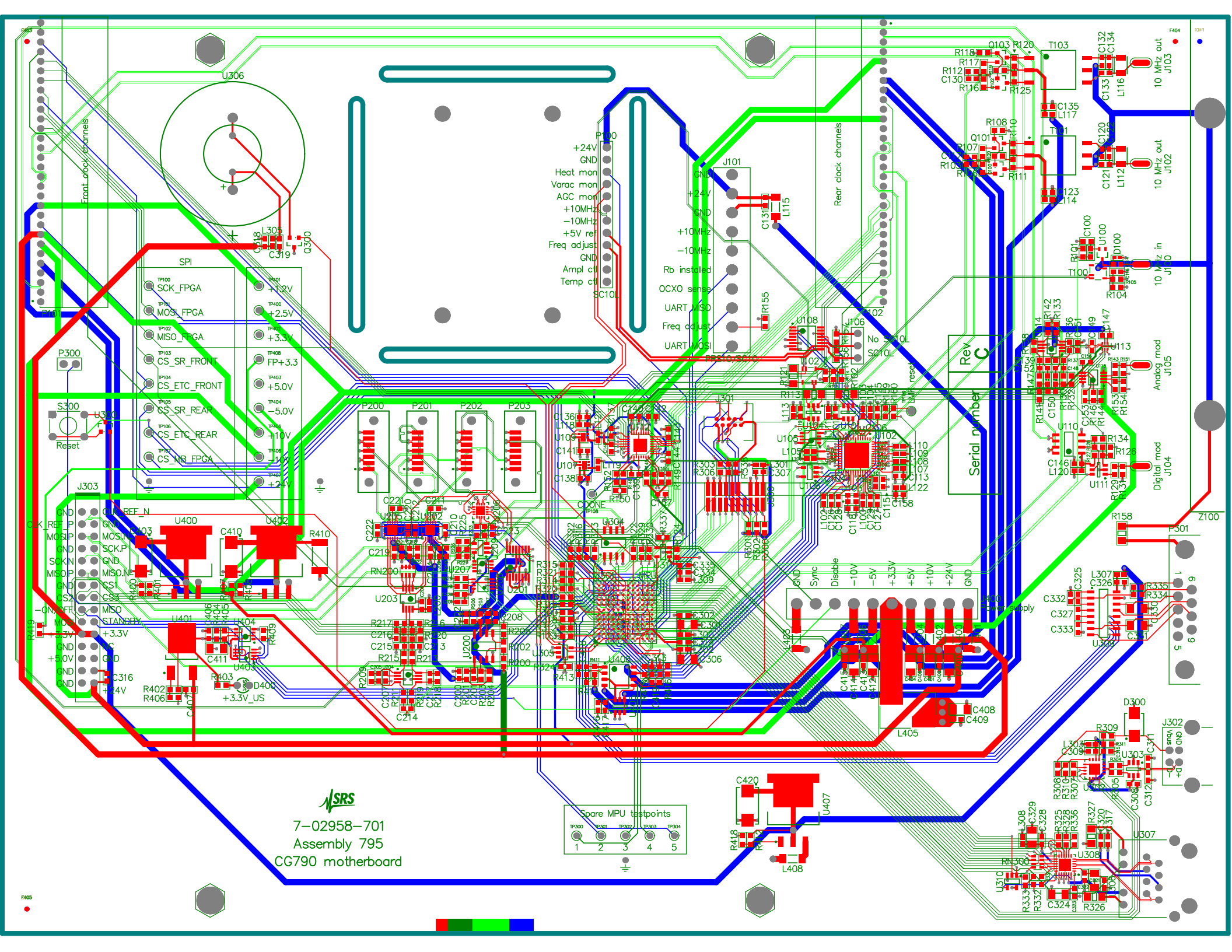
PC400 PCB

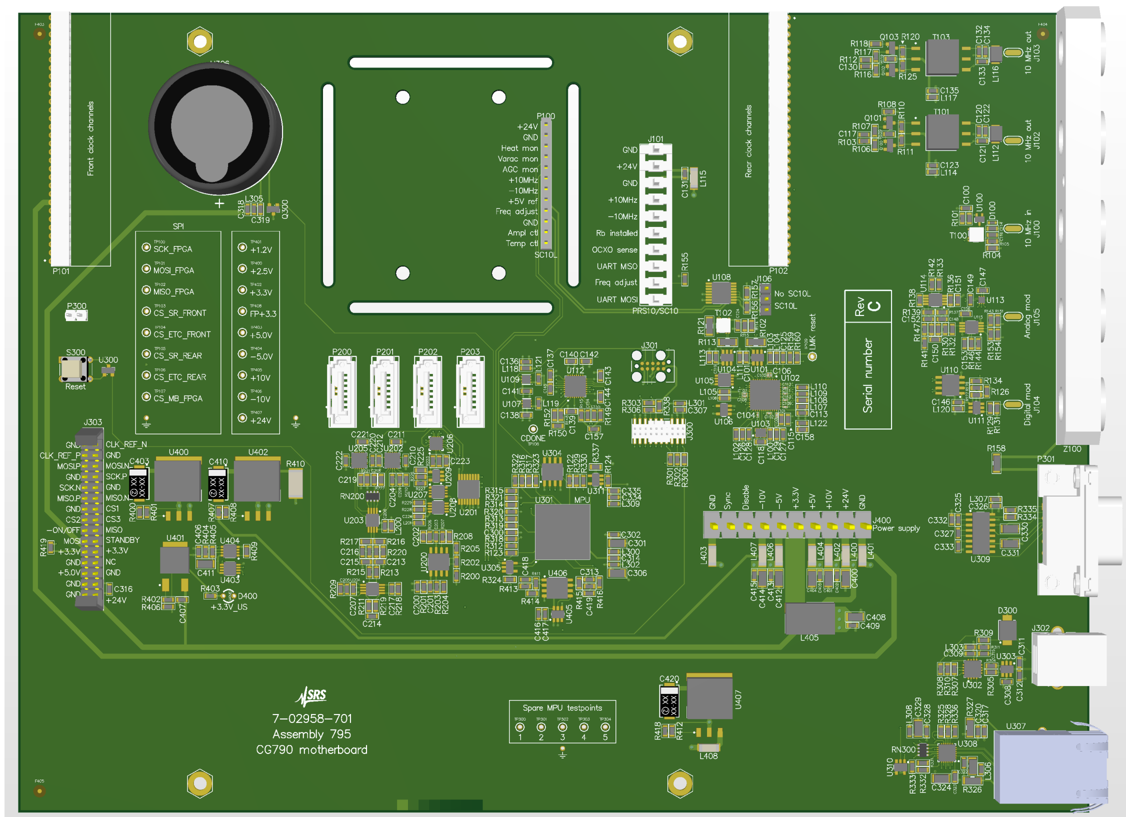
SRS

CG790 motherboard: power

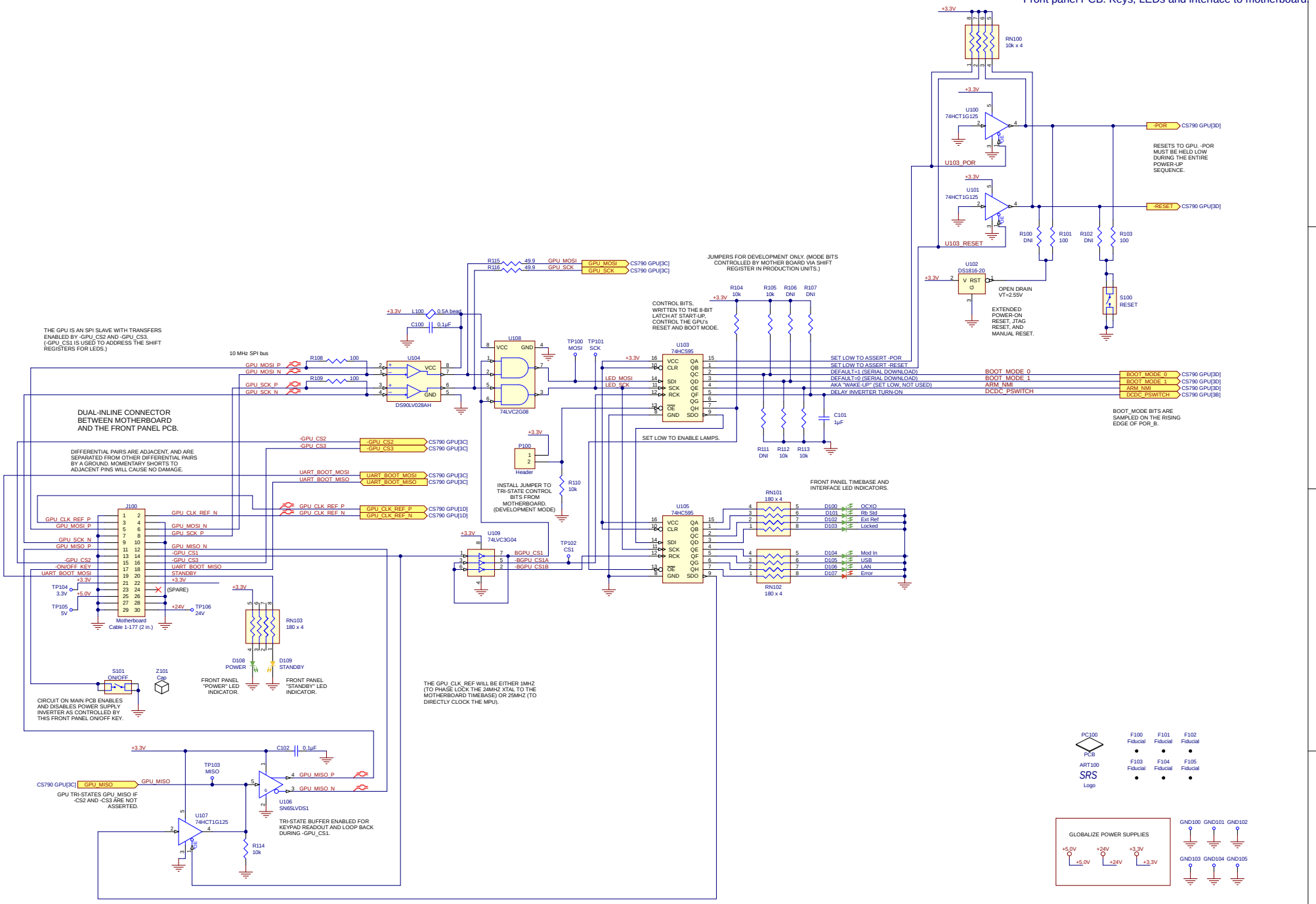
Assembly 795 Part number 7-02958 Revision C

9/18/2025 Designed by JRW Sheet 4 of 4


7–02958–701
Assembly 795
CG790 motherboard
Front clock channels
Rear clock channels
Serial number
Rev C
SPI
SCK_FPGA
MOSI_FPGA
MISO_FPGA
CS_SR_FRONT
CS_ETC_FRONT
CS_SR_REAR
CS_ETC_REAR
CS_MB_FPGA
+2.5V
+3.3V
FP+3.3
+5.0V
−5.0V
+10V
−10V
+24V
Reset
Spare MPU testpoints
10 MHz out J103
10 MHz out J102
10 MHz in J100
Analog mod J105
Digital mod J104
Disable
Sync
No SC10L
SC10L
Rb installed
OCXO sense
UART MISO
UART MOSI
Freq adjust
Heat mon
Varac mon
AGC mon
+10MHz
−10MHz
+5V ref
Ampl ctl
Temp ctl
+3.3V_US


7–02958–701
Assembly 795
CG790 motherboard
Front clock channels
Rear clock channels
Spare MPU testpoints
Serial number
Rev C
Power supply
Reset
SPI
10 MHz out
10 MHz in
Analog mod
Digital mod

Front panel PCB. Keys, LEDs and interface to motherboard.

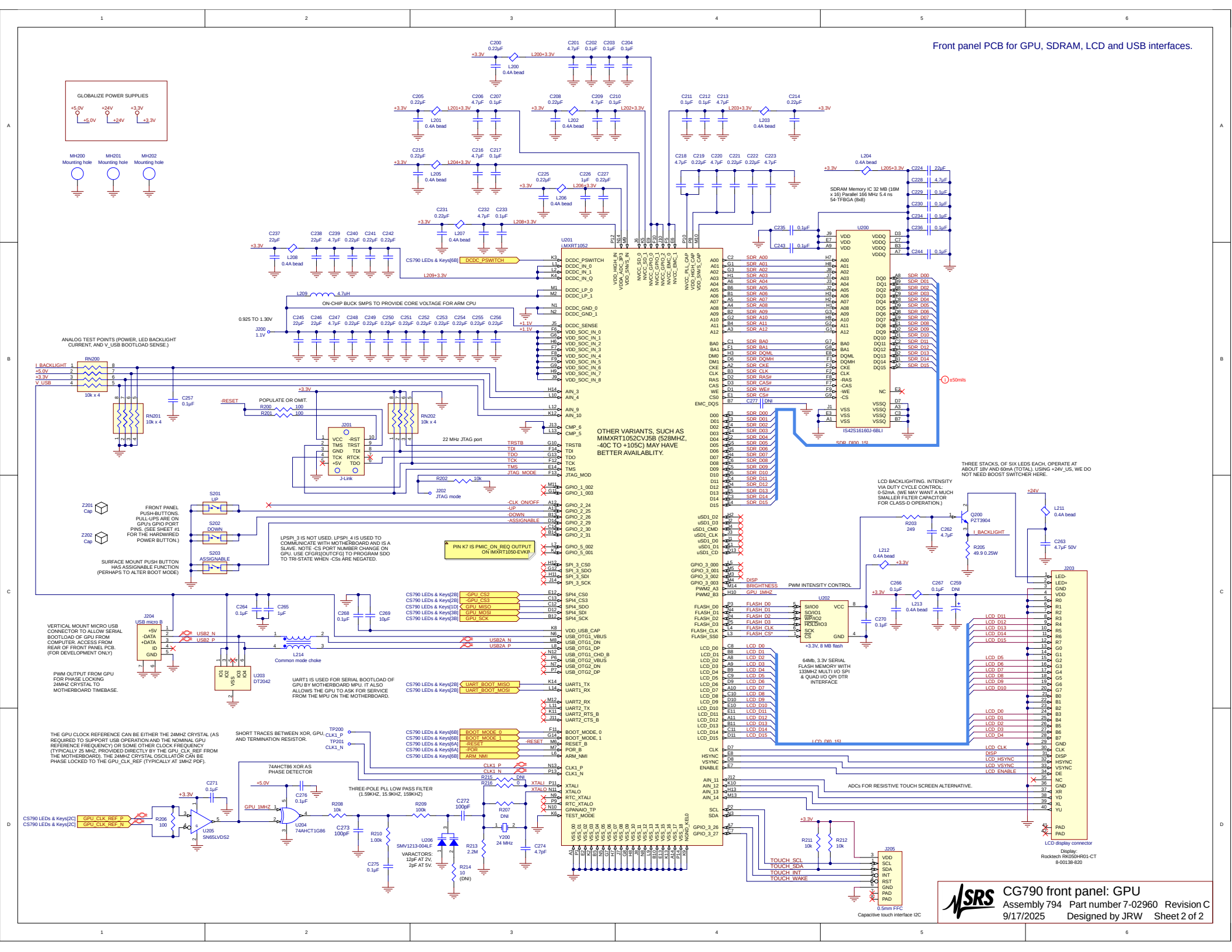


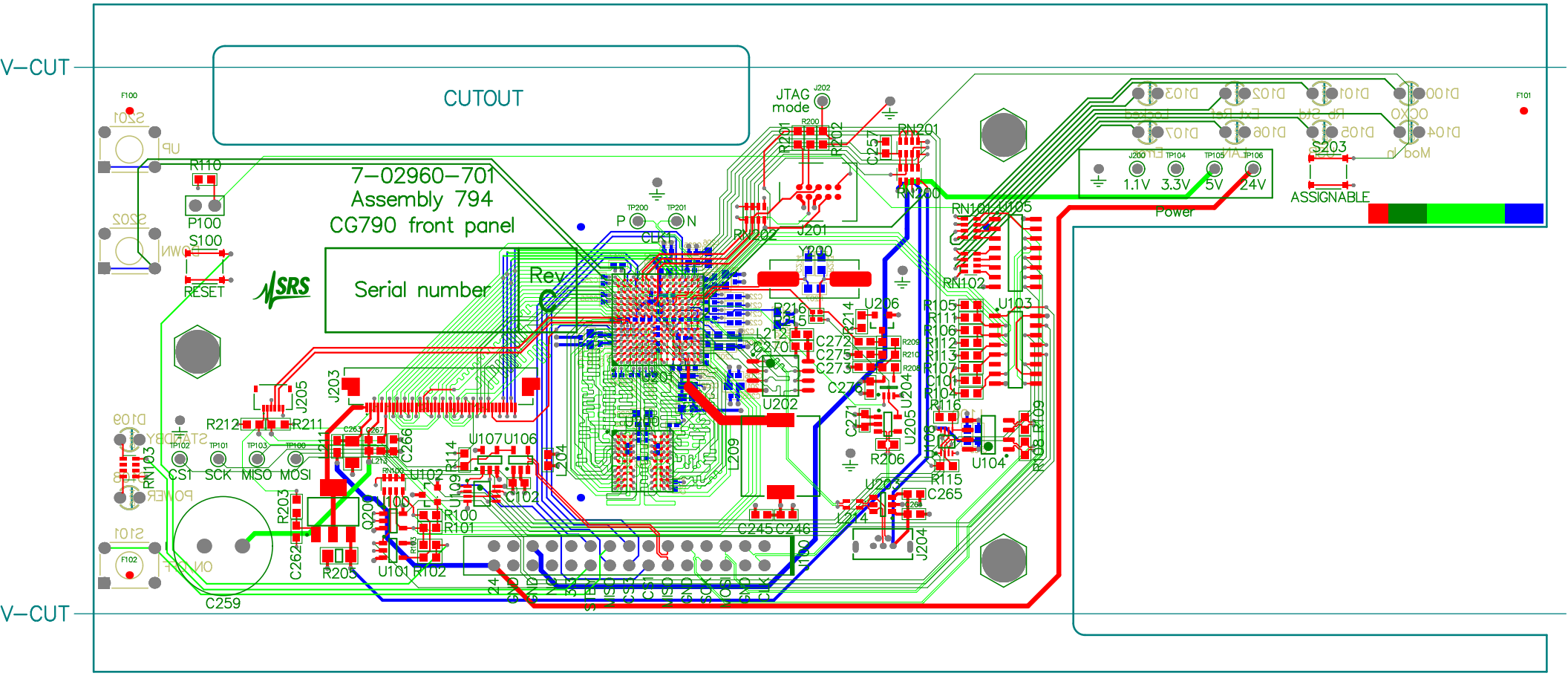
CG790 front panel: LEDs and keys

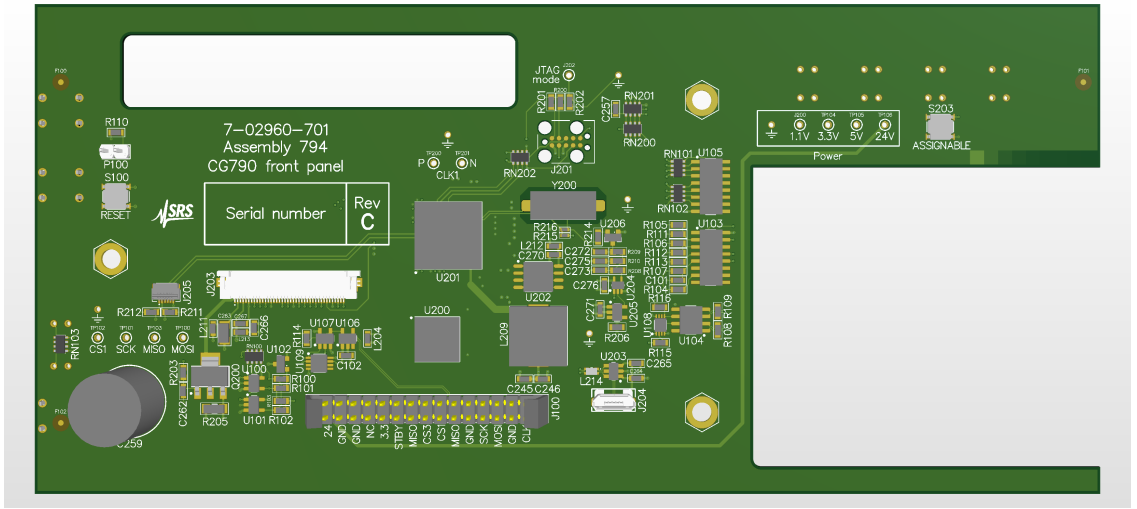
Assembly 794 Part number 7-02960 Revision C

9/17/2025 Designed by JRW Sheet 1 of 2

Front panel PCB for GPU, SDRAM, LCD and USB interfaces.




V-CUT
CUTOUT
7-02960-701
Assembly 794
CG790 front panel
Serial number
Rev C
JTAG mode
Power
1.1V
3.3V
5V
24V
ASSIGNABLE
RESET
CS1
SCK
MISO
MOSI
V-CUT


7-02960-701
Assembly 794
CG790 front panel
Serial number
Rev
C
JTAG mode
CLK1
Power
1.1V
3.3V
5V
24V
ASSIGNABLE
RESET
CS1
SCK
MISO
MOSI
24
GND
GND
NC
3.3
STBY
MISO
CS3
CS1
MISO
GND
SCK
MOS
GND
CL

+24VDC FROM OEM UNIVERSAL INPUT OFF-LINE SMPS.

REVERSE POLARITY PROTECTION (2A PER DIODE)

1x10 POSITION FEMALE SOCKET ON 0.156" PITCH FOR CONNECTION TO MOTHERBOARD.

J1 Header V 156 mil 1x4

D1 MBRS230LT3G
D2 MBRS230LT3G
D3 MBRS230LT3G

C1 4.7µF

J2 Header V 156 mil 1x10
+24V_US
+15V/+10V
+5.0V
+3.3V
-5.0V
-15V/-10V
-DISABLE
PS_SYNC

ART1 SRS Logo
PC1 PCB

MH1 Mounting hole
MH2 Mounting hole
MH3 Mounting hole
MH4 Mounting hole

F1 Fiducial
F2 Fiducial
F3 Fiducial

MB1 Mouse bites
MB2 Mouse bites
MB3 Mouse bites
MB4 Mouse bites

U1C NCS20072

+20/+14

INSTALL Z1 ON THIS HEADER FOR ±15VDC REGULATOR OUTPUTS.

INCREASE LM317 OUTPUT TO +15V WHEN HIGH VOLTAGE HEADER IS INSTALLED.

ALL FIVE REGULATORS ARE IN TO-220 PACKAGES AND ARE MOUNTED TO THE WALL OF THE THE POWER SUPPLY CHASSIS. TANTALUM OUTPUT CAPACITORS ARE USED FOR THEIR MODERATE ESR REQUIRED FOR REGULATOR STABILITY. SCHOTTKY DIODE PREVENT REVERSE BIASES ON POWER-UP.

P1 15V
Z1 Jumper

D4 ES2D
D6 ES2D

L1 22 µH

R2 33.2
C2 1000pF 2kV

C6 330µF
C5 4.7µF

U2 LM317AT
IN OUT ADJ

R3 210
R4 121
R5 845

C3 10µF
D5 MBRS230LT3G

+15V/+10V 1.5A

HIGH VOLTAGE, FAST RECOVERY DIODES USED HERE.

Snubbers absorb high-frequency ringing from diode switching

NO C_adjust IS NEEDED AS THERE IS VERY LITTLE INPUT RIPPLE AT LOW FREQUENCIES.

INSTALL Z1 ON THIS HEADER FOR ±10VDC REGULATOR OUTPUTS.

P2 10V

D7 ES2D
D8 ES2D

R6 33.2
C7 1000pF 2kV

C8 330µF
C9 4.7µF

L2 22 µH

-20/-14

U4 LM337
IN OUT ADJ

R12 121
R13 2.32k
R14 1.33k

C11 10µF
D9 MBRS230LT3G

-15V/-10V 1.5A

REDUCE LM337 OUTPUT TO -10V WHEN LOW VOLTAGE HEADER IS INSTALLED.

KICK-START FAN ON POWER-UP.

1.33x gain

THERMOSTATICALLY CONTROLLED FAN

U3 LM317L
IN ADJ OUT
(FOR LM5030)
+10.2V

R7 100.0
R10 715
C10 0.1µF

C4 4.7µF
+5.0V

R27 100k
R28 33.2k

+5.1V AT 25°C

U1B NCS20072

Q1 MJD243

J3 MTA-100

2-PIN HEADER FOR FAN
Mating connector: 1-00472-112
Fan: 0-01181-070 (12V 50 mA)

R1 100k
R25 100k

THERMISTOR, 0603 PACKAGE. ABOUT −5.1%/°C. PLACE NEXT TO PCB MOUNTING HOLE.

R8 100k thermistor
RN2A 100k x 4

R9 237k
SET GAIN (dV/dT)

MATCH GAIN SETTING RESISTOR FOR 25°C INTERCEPT.

R15 237k
RN2D 100k x 4
RN2B 100k x 4
RN2C 100k x 4 (NC)

U1A NCS20072

Leads on U1's TSSOP package were too close together for 2 oz copper. Changed to SO-8.

INVERTER LTSpice SIMULATION AT "Power supply Rev G.asc"

SNUBBERS ARE ON ALL SECONDARIES.

T1 Transformer
3T 7T 10T 7T 3T 10T 4T 4T 3T 3T

R11 33.2
C30 1000pF 2kV
C31 1000pF 2kV
R26 33.2

C16 4.7µF
C17 330µF

D10 MBRS230LT3G
D12 MBRS230LT3G
D13 MBRS230LT3G
D14 MBRS230LT3G
D16 MBRS230LT3G
D17 MBRS230LT3G

L3 10 µH
L4 10 µH

R16 33.2
R17 33.2
C12 1000pF 2kV
C18 1000pF 2kV

SNUBBERS

+8V
-8V

C15 330µF
C19 330µF
C13 4.7µF
C20 4.7µF

U5 LM1085IT-5.0
U6 LM2990T-5.0
IN OUT GND

C14 10µF
C21 10µF

D11 MBRS230LT3G
D15 MBRS230LT3G

+5.0V 3A
-5.0V 1.8A

SCHOTTKEY DIODES HEAT SUNK TO GROUND PLANE.

R18 33.2
C23 1000pF 2kV

SNUBBERS

L5 10 µH

+5.9V

C24 330µF
C25 4.7µF

U8 LM1085IT-ADJ
IN OUT ADJ
Out-1.25V

R29 124
R30 210

C26 10µF
D20 MBRS230LT3G

+3.3V 3A

Increasing R30 by 5 ohms raises regulator output by 50 mV.

R30 (ohms)	Output (V)
200	3.266
205	3.316
210	3.367
215	3.417

+10.2V REGULATOR REDUCES POWER DISSIPATION IN LM5030.

C29 0.1µF

U7 LM5030
VIN VCC
RT/SYNC OUT1
VFB OUT2
COMP CS
SS GND
PAD

SLOW ON, FAST OFF. GATE DRIVE RESISTORS HAVE ABOUT 70mA(RMS) CURRENT. (CAN'T USE 0603 PART!)

D18 MBRS230LT3G
D19 MBRS230LT3G

R19 33.2
R20 33.2

Q3 STP19NF20
Q4 STP19NF20

TO-220 CHASSIS MOUNTED N-CHANNEL MOSFETS.

Original part (100V): 3-00283-340 (IRF530)
Alternate part (200V): 3-02856-333 (STP19NF20)

PS_SYNC PULSE GOES HIGH FOR 15-150ns AT A RATE OF 200kHz.

C22 100pF
PS_SYNC
R21 40.2k

-DISABLE

-DISABLE IS OPEN DRAIN THAT PULLS LOW TO TURN OFF INVERTER.

C27 0.1µF

SYNCHRONOUS GATE DRIVER OPERATES NEAR 100% DUTY CYCLE (135ns DEADTIME) AND PROVIDES OVER CURRENT PROTECTION.

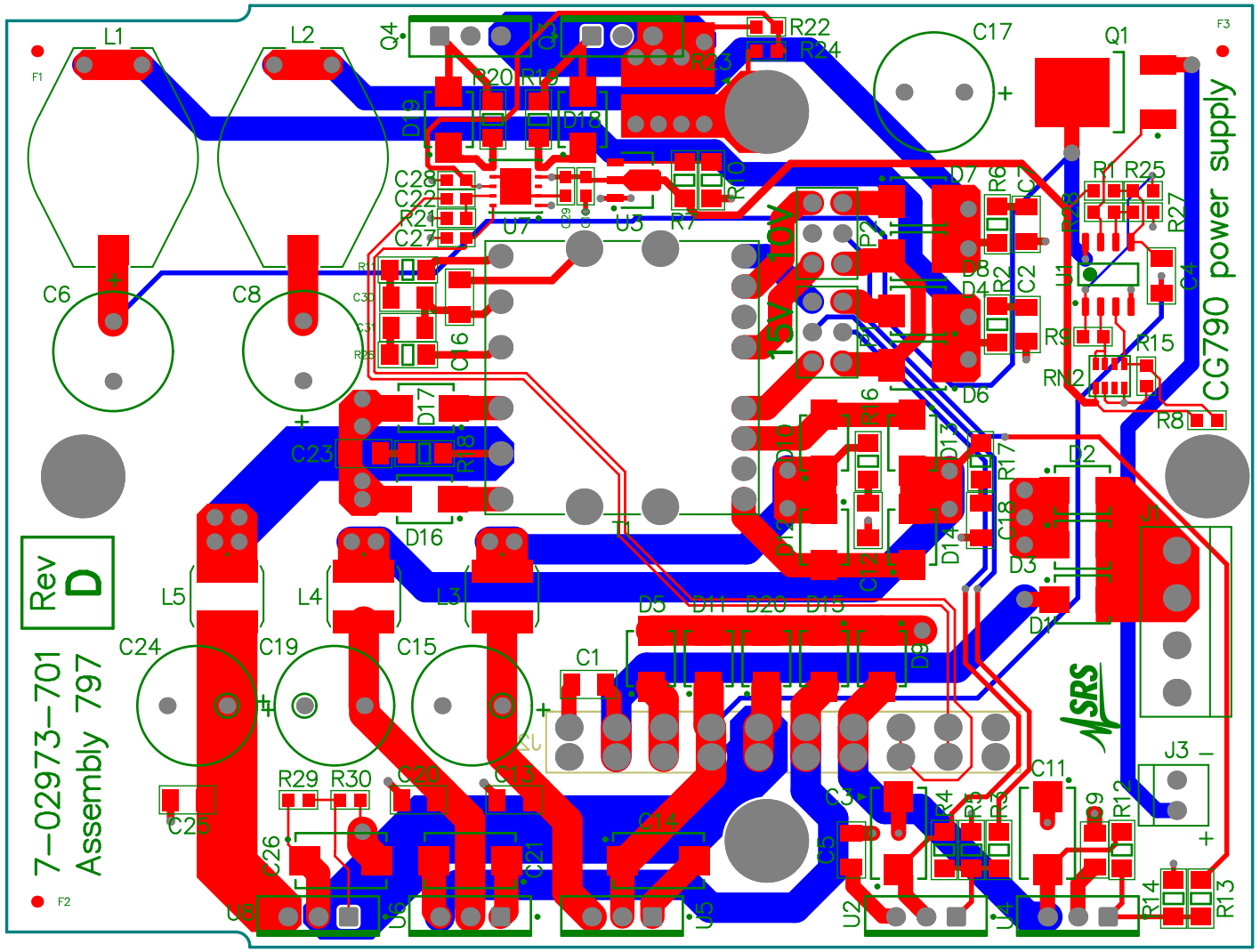
530 kHz LPF

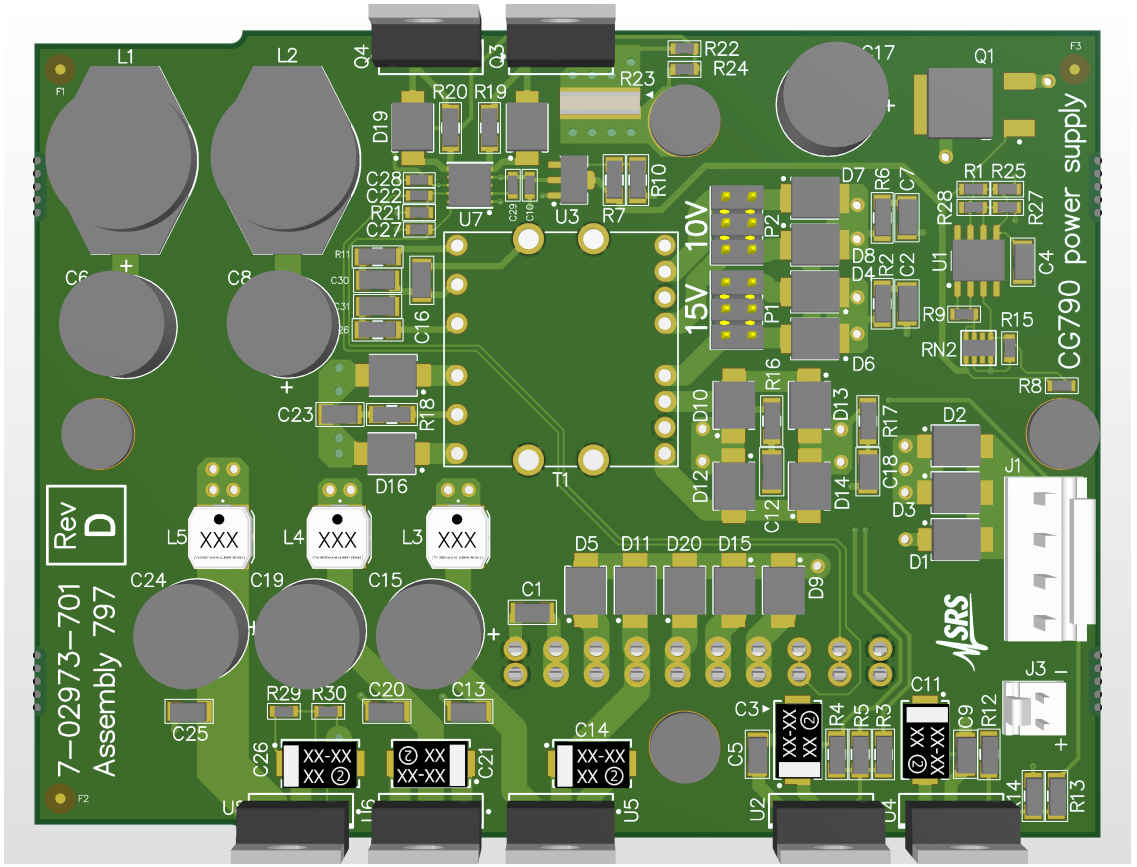
C28 1000pF
R24 332

CURRENT LIMIT ADJUSTMENT

R22 301
R23 0.15

CG790 power supply
Assembly 797 Part number 7-02973 Revision D
9/11/2025 Designed by JRW Sheet 1 of 1


CG790 power supply
Rev D
7-02973-701
Assembly 797
15V
10V
L1
L2
L3
L4
L5
C6
C8
C17
Q1
Q4
R22
R24
R23
R20
R19
C28
C22
R21
C27
U7
U5
R7
D7
D8
D4
D6
R1
R25
R27
C4
C2
U1
R9
R15
RN2
R8
C16
D17
C23
D16
R16
D10
D13
R17
D2
D3
C18
J1
D5
D11
D20
D15
D1
C1
C24
C19
C15
C12
C13
C20
R29
R30
C25
C26
C21
C14
C3
C11
J3
R4
R12
R14
R13
U8
U9
U2
U4
F1
F2
F3

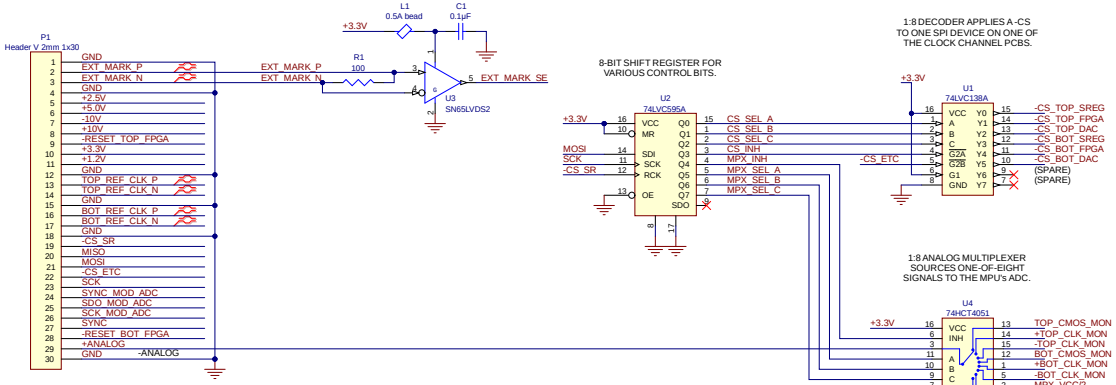

CG790 power supply
7-02973-701
Assembly 797
Rev
D
15V
10V
SRS
L1
L2
L3
L4
L5
Q1
Q3
Q4
U1
U2
U3
U4
U5
U7
T1
J1
J3
C1
C2
C3
C4
C5
C6
C7
C8
C9
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D19
D20
P1
P2
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R27
R28
R29
R30
RN2
XXX
XX-XX

VERTICAL INTERFACE BOARD WHICH CONNECTS TWO CLOCK CHANNELS (FRONT OR REAR) TO THE MOTHERBOARD.

ONLY THREE 30-PIN HEADERS WILL BE INSTALLED IN LOCATIONS THAT ARE DIFFERENT FOR FRONT AND REAR VERTICAL PCBs.

CONNECTOR TO THE MOTHERBOARD. (THIS 30-PIN HEADER WILL ALWAYS BE INSTALLED.)

+/-EXT_MARK (LVDS) IS THE DISCRIMINATED LEVEL FROM THE REAR-PANEL EXTERNAL MODULATION INPUT FOR BLANKING, POLARITY INVERSION, ETC.



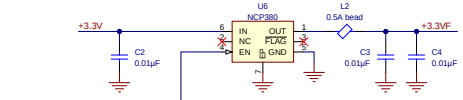
8-BIT SHIFT REGISTER FOR VARIOUS CONTROL BITS.

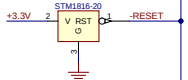
1:8 DECODER APPLIES A -CS TO ONE SPI DEVICE ON ONE OF THE CLOCK CHANNEL PCBS.

1:8 ANALOG MULTIPLEXER SOURCES ONE-OF-EIGHT SIGNALS TO THE MPU's ADC.

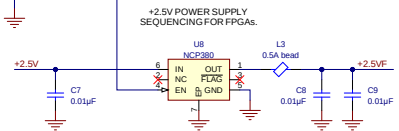
PIN ASSIGNMENTS MADE SO THAT NOISY SIGNALS ARE SEPARATED FROM SENSITIVE SIGNALS. AND, GENERALLY, THERE'D BE NO DAMAGE FROM A BRIEF SHORT BETWEEN ADJACENT PINS.

+3.3V POWER SUPPLY SEQUENCING FOR FPGAs.

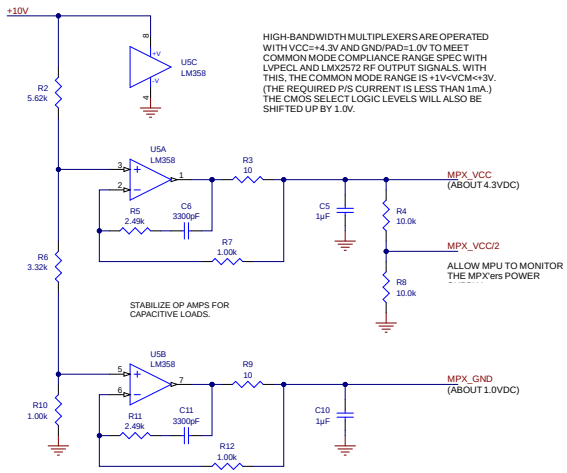




+2.5V POWER SUPPLY SEQUENCING FOR FPGAs.



HIGH-BANDWIDTH MULTIPLEXERS ARE OPERATED WITH VCC=+4.3V AND GND/PAD=1.0V TO MEET COMMON MODE COMPLIANCE RANGE SPEC WITH LVPECL AND LMX2572 RF OUTPUT SIGNALS. WITH THIS, THE COMMON MODE RANGE IS +1V<VCM<+3V. (THE REQUIRED P/S CURRENT IS LESS THAN 1mA.) THE CMOS SELECT LOGIC LEVELS WILL ALSO BE SHIFTED UP BY 1.0V.



ART1 Logo

PC1 PCB

MB1 Mouse bites

MB3 Mouse bites

MB2 Mouse bites

MB4 Mouse bites

F1 Fiducial

F2 Fiducial

F3 Fiducial

POPULATE FOR FRONT VERTICAL PCB

POPULATE THESE TWO HEADERS FOR VERTICAL PCBs BUILT TO CONNECT FRONT PANEL CLOCK OUTPUTS.

HEADER FOR CLOCK#1. (DNI ON REAR VERTICAL PCB.)

P2
Clock 1 - Front

1	GND
2	-TOP_CLK_MON
3	+TOP_CLK_MON
4	-CS_TOP_DAC
5	-RESET_TOP_FPGA
6	+5.0V
7	-10V
8	+10V
9	MPX_GND
10	MPX_VCC
11	+3.3V
12	+3.3VF
13	+1.2V
14	+2.5VF
15	GND
16	TOP_REF_CLK_P
17	TOP_REF_CLK_N
18	GND
19	-CS_TOP_SREG
20	MISO
21	MOSI
22	-CS_TOP_FPGA
23	SCK
24	SYNC_MOD_ADC
25	SDO_MOD_ADC
26	SCK_MOD_ADC
27	EXT_MARK_SE
28	SYNC
29	TOP_CMOS_MON
30	GND

HEADER FOR CLOCK#2. (DNI ON REAR VERTICAL PCB.)

P4
Clock 2 - Front

1	GND
2	-BOT_CLK_MON
3	+BOT_CLK_MON
4	-CS_BOT_DAC
5	-RESET_BOT_FPGA
6	+5.0V
7	-10V
8	+10V
9	MPX_GND
10	MPX_VCC
11	+3.3V
12	+3.3VF
13	+1.2V
14	+2.5VF
15	GND
16	BOT_REF_CLK_P
17	BOT_REF_CLK_N
18	GND
19	-CS_BOT_SREG
20	MISO
21	MOSI
22	-CS_BOT_FPGA
23	SCK
24	SYNC_MOD_ADC
25	SDO_MOD_ADC
26	SCK_MOD_ADC
27	EXT_MARK_SE
28	SYNC
29	BOT_CMOS_MON
30	GND

SURROUND REF_CLK WITH GROUNDS.

POPULATE FOR REAR VERTICAL PCB

POPULATE THESE TWO HEADERS FOR VERTICAL PCBs BUILT TO CONNECT REAR PANEL CLOCK OUTPUTS.

HEADER FOR CLOCK#3. (DNI ON FRONT VERTICAL PCB.)

P3
Clock 3 - Rear

1	GND
2	-TOP_CLK_MON
3	+TOP_CLK_MON
4	-CS_TOP_DAC
5	-RESET_TOP_FPGA
6	+5.0V
7	-10V
8	+10V
9	MPX_GND
10	MPX_VCC
11	+3.3V
12	+3.3VF
13	+1.2V
14	+2.5VF
15	GND
16	TOP_REF_CLK_P
17	TOP_REF_CLK_N
18	GND
19	-CS_TOP_SREG
20	MISO
21	MOSI
22	-CS_TOP_FPGA
23	SCK
24	SYNC_MOD_ADC
25	SDO_MOD_ADC
26	SCK_MOD_ADC
27	EXT_MARK_SE
28	SYNC
29	TOP_CMOS_MON
30	GND

HEADER FOR CLOCK#4. (DNI ON FRONT VERTICAL PCB.)

P5
Clock 4 - Rear

1	GND
2	-BOT_CLK_MON
3	+BOT_CLK_MON
4	-CS_BOT_DAC
5	-RESET_BOT_FPGA
6	+5.0V
7	-10V
8	+10V
9	MPX_GND
10	MPX_VCC
11	+3.3V
12	+3.3VF
13	+1.2V
14	+2.5VF
15	GND
16	BOT_REF_CLK_P
17	BOT_REF_CLK_N
18	GND
19	-CS_BOT_SREG
20	MISO
21	MOSI
22	-CS_BOT_FPGA
23	SCK
24	SYNC_MOD_ADC
25	SDO_MOD_ADC
26	SCK_MOD_ADC
27	EXT_MARK_SE
28	SYNC
29	BOT_CMOS_MON
30	GND

TOP

BOTTOM

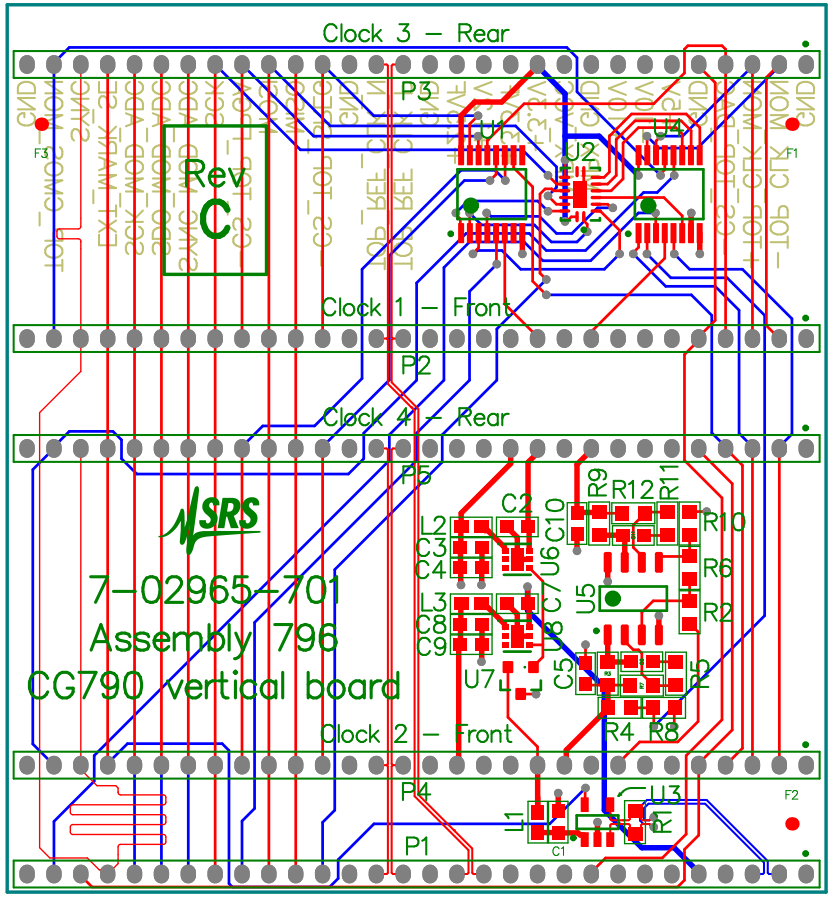
PIN ASSIGNMENTS MADE SO THAT NOISY SIGNALS ARE SEPARATED FROM SENSITIVE SIGNALS. AND, GENERALLY, THERE'D BE NO DAMAGE FROM A BRIEF SHORT BETWEEN ADJACENT PINS.

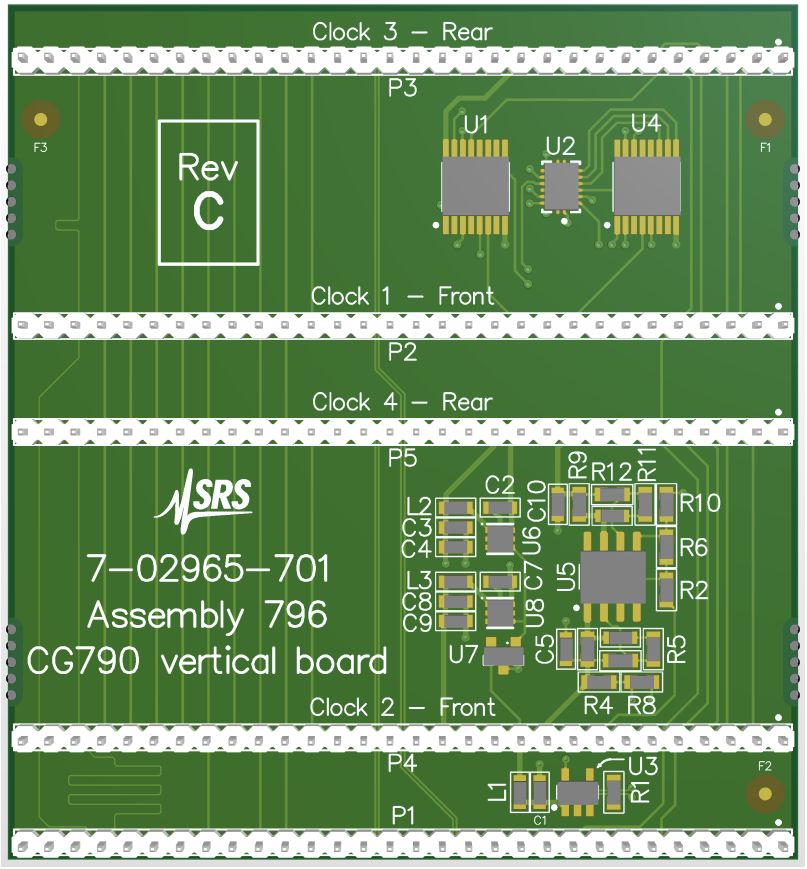
SRS

CG790 vertical PCBs

Assembly 796 Part number 7-02965 Revision C

9/17/2025 Designed by JRW Sheet 1 of 1


Clock 3 – Rear
P3
Rev
C
U1
U2
U4
Clock 1 – Front
P2
Clock 4 – Rear
P5
SRS
7–02965–701
Assembly 796
CG790 vertical board
C2
L2
C3
C4
L3
C8
C9
U6
C10
C7
U5
U7
R9
R12
R11
R10
R6
R2
C5
R4
R8
Clock 2 – Front
P4
P1
U3
C1
F1
F2
F3



Distribution in the UK & Ireland

Characterisation, Measurement & Analysis

Lambda Photometrics Limited
Lambda House Batford Mill
Harpenden Herts AL5 5BZ
United Kingdom
E: info@lambdaphoto.co.uk
W: www.lambdaphoto.co.uk
T: +44 (0)1582 764334
F: +44 (0)1582 712084